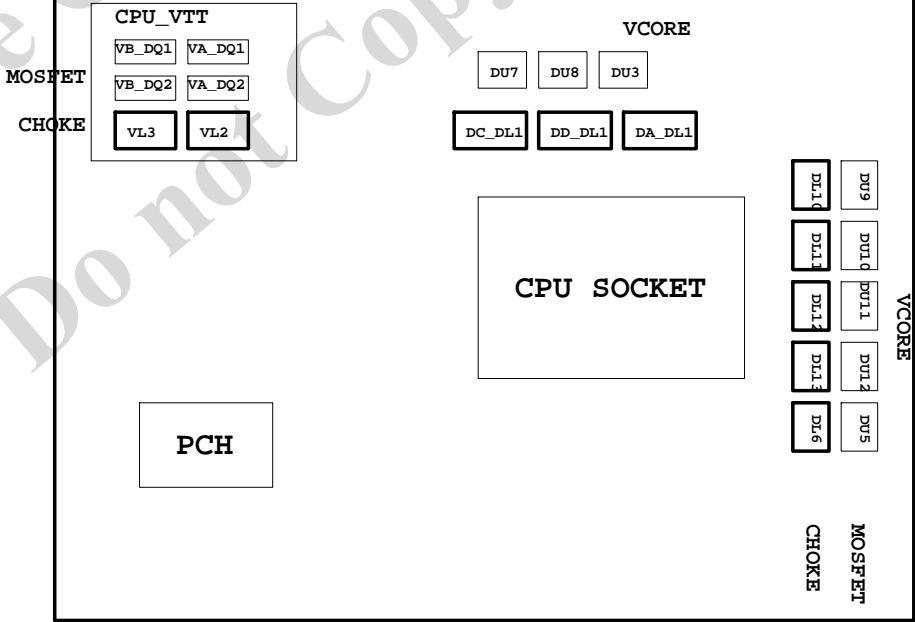


SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1155-A
05	CPU_LGA1155-B
06	CPU_LGA1155-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS*16 SLOT
15	PCI EXPRESS*8 SLOT
16	PCI EXPRESS*16/*8 SWITCH
17	PCI EXPRESS*1 SLOTS X3
18	PCI EXPRESS*4 SLOT
19	IT8892
20	PCI SLOT 1
21	HDMI/DVI/USB3.0
22	MSATA
23	Dual BIOS / TPM CONNECT
24	ALC889
25	REAR AUDIO JACK
26	VCORE PWM_IR3567
27	VCORE PWM_IR3567

28	VCORE PWM_IR3570
29	DDR / CPU_VTT MOS
30	DISCRETE POWER
31	VCCSA POWER
32	I/O ITE8728
33	COM,-PHOT,RUSB
34	FP,FUSB
35	ATX POWER, CLOCK GEN
36	HWM,KB/MS , FAN CTRL
37	ARTHEROS AR8161/AR8151
38	MARVELL 9172
39	NCT3933U
40	VIA VL800 USB3.0
41	TABLE LIST



GA-Z77X-D3H
Component value change history

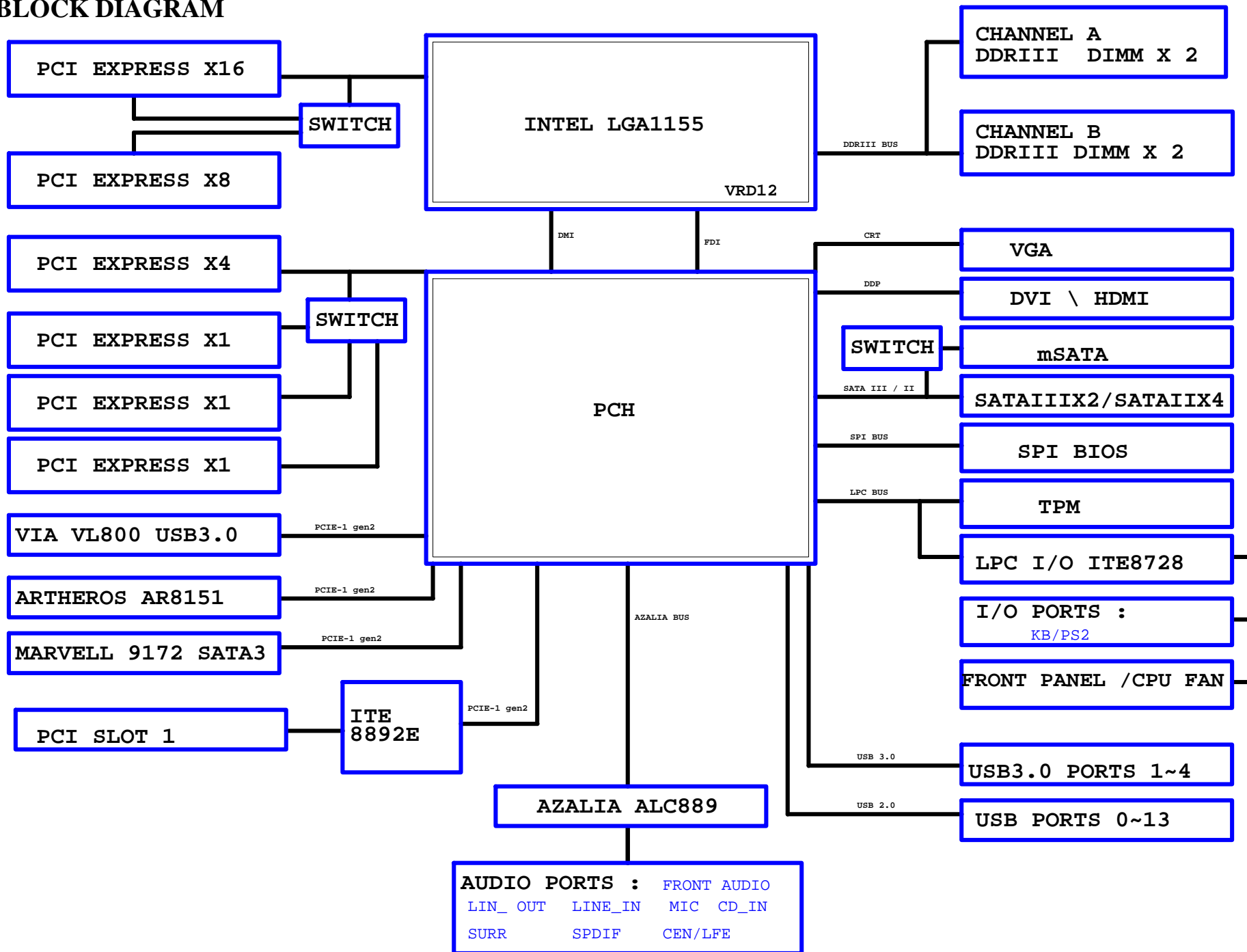
Data	Change Item	Reason
2011/12/02	1.First BOM. (GA-Z77X-D3H-01_20111125_1000-BOM.DSN)	
2012/01/03	1.PCH==>10HB1-030Z77-10R 2.PCH_HS==>12SP2-S05511-01R 3.ADD NR100 4.EMI ADD BC330 5.ADD PI3PCIE2415 FOR PCIEX4 SW TO X1 6.REMOVE DUAL BIOS SW 7.AUDIO CONNECT CHANGE TO 11NR6-403025-61R 8.REMOVE SURR BACK 9.DRAT2,DART3,MART3==>47K/1/4/S 10.DAR44,DAR15,MAR185==>0 OHM 11.ADD VA_DR2 FOR漏電 12.REMOVE DA_Q2,DB_DQ2==>DA_DQ3,DB_DQ3 13.後窗USB/USB_LAN CONNECT CHANGE TO USB3.0	9MZ77XD3H-00-02
2012/01/13	Modify 1.MAR149,DAR51,DAR1,24.9/4/1變更爲'100/4/1 2.DART2,DART3,MART3,47K/1/4/S變更爲47K/1/4/S/[10RH3-004702-21R] 3.MAC361,DAC24,DAC1,1N/4/X7R/50V/K變更爲3.3n/4/X7R/50V/K 4.MAR151,DAR54,DAR2,24.9/4/1變更爲0/4 Add 5..R5409,R5413,10K/4/1 6.R5412,R5408,45.3K/4/1 7.DAR82,0/4 8.C2068,C2069,0.1u/4/X7R/16V/K 9.Q668,Q670,2N7002/SOT23/25pF/5 10.U219,LM358DR/SO8 11.R5414,R5410,1.65K/4/1 12.RS1,RS2,100K/1/4/S 13.R_USB30_1,USB/18P/BU/OS/RA/D/2/HR 14.DB_DQ2,DA_DQ2,DF_DQ3,DE_DQ3,DD_DQ3,DC_DQ3,RJK0393DPA-0G/N/4.3m/PPAKSO-8 15.R5411,R5415,1K/4/1 16.RHC3,GBC28,LAC33,47p/4/NPO/50V/J Delete 1.UCR29,'8.2K/4 2.UCR25,'6.04K/4/1 3.UCQ2,'2N7002/SOT23/25pF/5 4.R_USB30,'USB/18P/BU/OS/RA/D/2/HR 5.U8,'NCT3931U-2/SOT23-8	9MZ77XD3H-00-10A
2012/01/13	1.DA_DR11,DC_DR11,DE_DR11,DZ_DR11,1/4 change to 0/4 2.FAN1/2/3 change to SYS_FAN1/2/3,V-A AMP WF 1*4P PINREX	9MZ77XD3H-00-10B
2012/01/31	1.R5410,R5414,1.65K change to 3.65K	9MZ77XD3H-00-10C
2012/02/03	Modify 1.R5410,'3.65K/4/1變更爲'1.65K/4/1 2.DAR6,'5.36K/4/1變更爲'5.1K/4/1 3.DY_DL1,DZ_DL1,VL2,DA_DL1,DB_DL1,DC_DL1,DE_DL1,DF_DL1, '0.8uH/35A/INC109/F/D變更爲'0.36uH/38A/IGC109/FS/D 4.DAR45,DAR40,'1.54K/4/1變更爲'1.74K/4/1 5.DAR5,DAR8,'4.12K/4/1變更爲'4.75K/4/1 6.R5414,'3.65K/4/1變更爲'2.49K/4/1 7.DAR13,DAR36,DAR25,DAR59,DAR62,DAR75,DAR21,2K/4/1變更爲1.2K/4/1 8.DAR42,'2.05K/4/1變更爲2.37K/4/1 Add 1.DZ_DR10,DE_DR10,DC_DR10,DA_DR10,'0/4 Delete 1.DE_DR11,DC_DR11,DA_DR11,DZ_DR11,'0/4	9MZ77XD3H-00-10D
2012/02/07	Modify 1.DAR6,5.1K/4/1 change to 5.49K/4/1	9MZ77XD3H-00-10E
2012/03/13	1.Add MR34,MR35==>0 ohm 2.Remove UCU1 VIA USB30 EEPROM 3.Delete OR48,Add OR51 for MB_ID3	9MZ77XD3H-00-10K
2012/03/22	1.Add UCU1 EEPROM	9MZ77XD3H-00-10L
2012/03/23	1.PCB change to 1.03	9MZ77XD3H-00-10Q

Circuit or PCB layout change

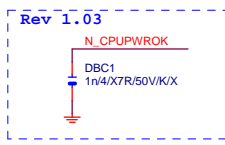
DATE	Change Item	Reason
2011/11/30	1.First SCH. (GA-Z77X-D3H-01_20111125_1000.DSN)	REV 0.1
	(Change from Z77X-UD3H-01A_1124_EBOM.DSN)	
2012/01/02	1.PARN2 change to 0/8P4R/4/X 2.ADD PI3PCIE2415 FOR PCIEX4 SW TO X1 3.REMOVE DUAL BIOS SW 4.AUDIO CONNECT CHANGE TO 11NR6-403025-61R (WITH SPDIF) 5.REMOVE SURR BACK 6.CPU_VTT ADD DUAL POWER 防漏電 7.VL2轉方向 8.ADD VIA VL800 USB3.0 9.後窗USB/USB_LAN CONNECT CHANGE TO USB3.0 10.ADD ATX POWER LOAD RESISTOR 11.SYS_FAN1/2/3 RENAME TO FAN1/2/3	REV 0.2
2012/01/13	1.Add PWM 3VDUAL input 2.Add GBC28 3.Add 2組 VR_HOT control線路 4.DAR53,DAR55,MAR148 CHANGE TO R0402-2 5.R_USB30 rename to R_USB30_1	REV 1.0
2012/01/19	1.FAN1/2/3 rename to SYS_FAN1/2/3	Rev 1.01
2012/02/22	1.DDR T型走線 2.Add MR34,MR35	Rev 1.02
2012/03/21	1.縮短DDR slot 間距 for O.C. 2.Add DBC1 for EMI ESD improve	Rev 1.03
2012/05/28	1.版本改爲 Rev 1.1 2.FB2,FB3,FB4, FB0603-RH change to FB0402-RH 3.msATA MINI_PCIE52P-A-1 change to MINI_PCIE52P-B-1-COLAY 4.ATX_12V change to ATX_12V_2X4 5.CFB1,FB6,NFB3,NFB4,NFB5,NFB6,LAFB2,LAFB3,RHFB2,change to 0402 6.Add R854,BC36	

Gigabyte Technology			
Title BOM & PCB MODIFY HISTORY			
Size	Document Number	GA-Z77X-D3H	
Custom			Rev 1.1
Date:	Tuesday, July 10, 2012	Sheet	2 of 41

BLOCK DIAGRAM



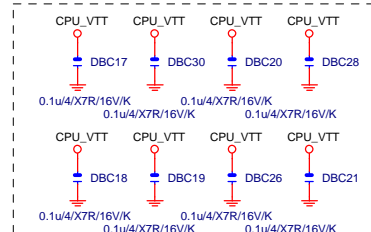
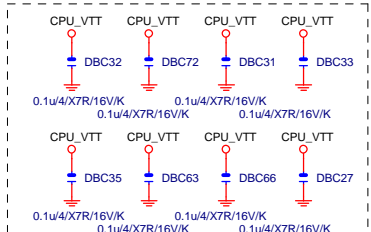
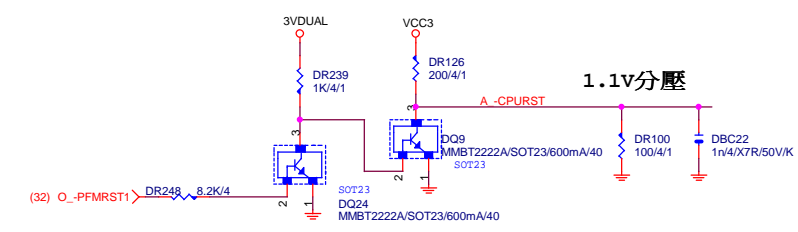
CFG5:1: 1X16 PEG
CFG5:0: 2X8 PEG

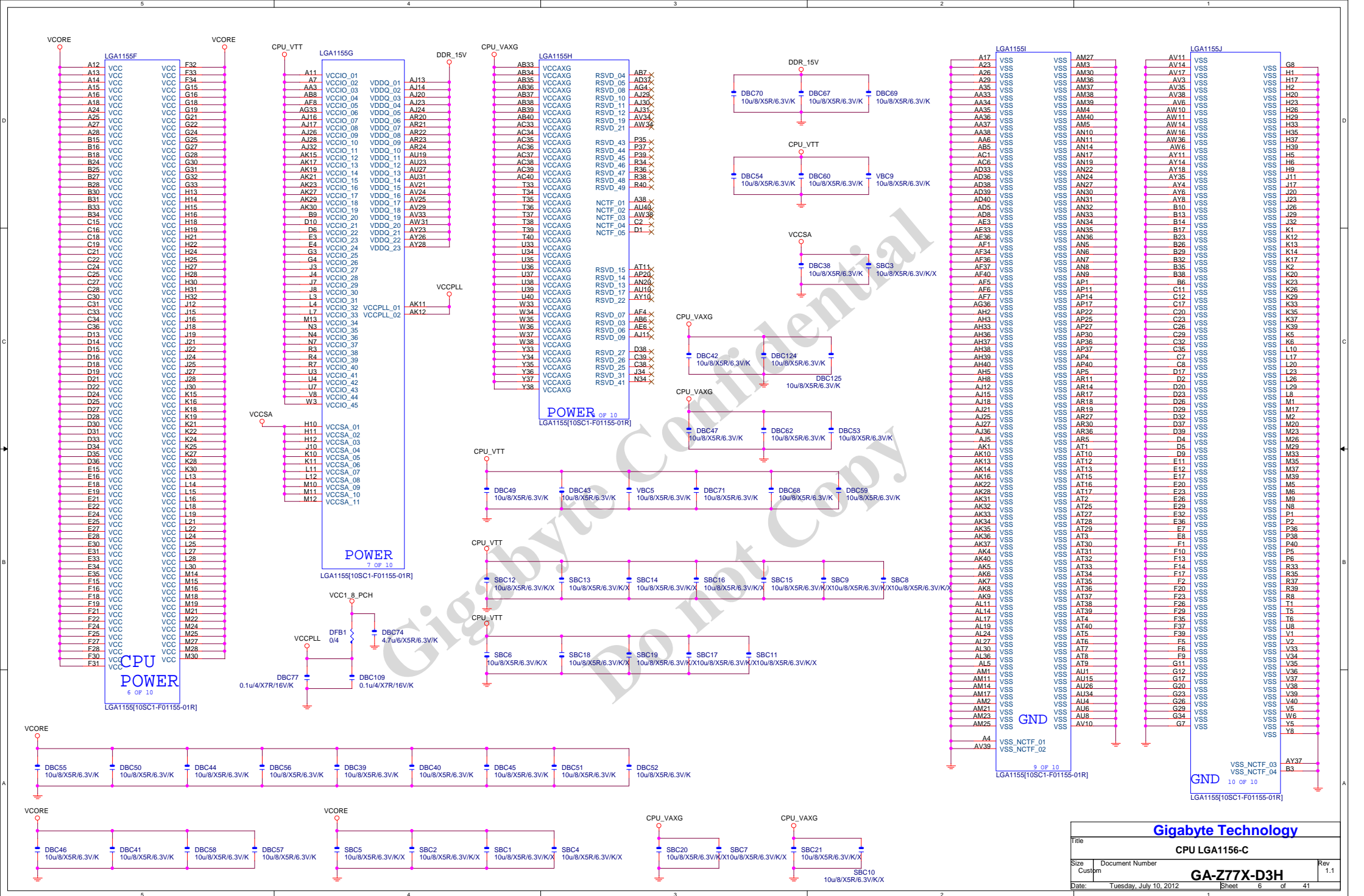


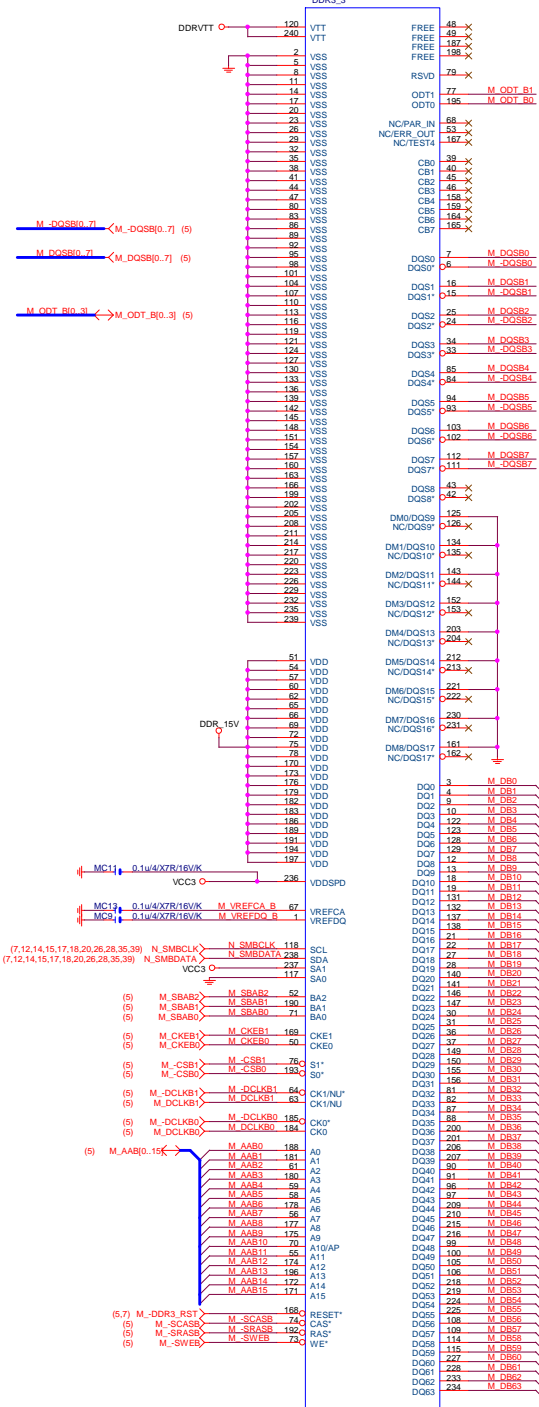
CFG	H	L	NOTE
0	RSVD	RSVD	RSVD
1	RSVD	RSVD	RSVD
2	NORM	Reverse	LANE REVERSAL[0].x16
3	RSVD	RSVD	RSVD
4	RSVD	RSVD	RSVD
7	RSVD	RSVD	RSVD
8	RSVD	RSVD	RSVD
9	RSVD	RSVD	RSVD
10	RSVD	RSVD	RSVD
11	RSVD	RSVD	RSVD
12	RSVD	RSVD	RSVD
13	RSVD	RSVD	RSVD
14	RSVD	RSVD	RSVD
15	RSVD	RSVD	RSVD
16	RSVD	RSVD	RSVD
17	RSVD	RSVD	RSVD

CFG6	CFG5	PCIE CONFIG
1	1	1X16, Default
0	0	RSVD
0	1	RSVD
0	0	X8_X4_X4

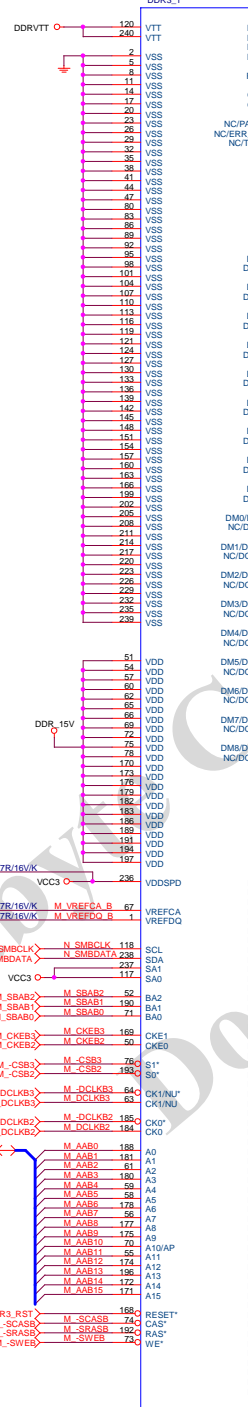
CFG 0-17 all internal PULL-UP



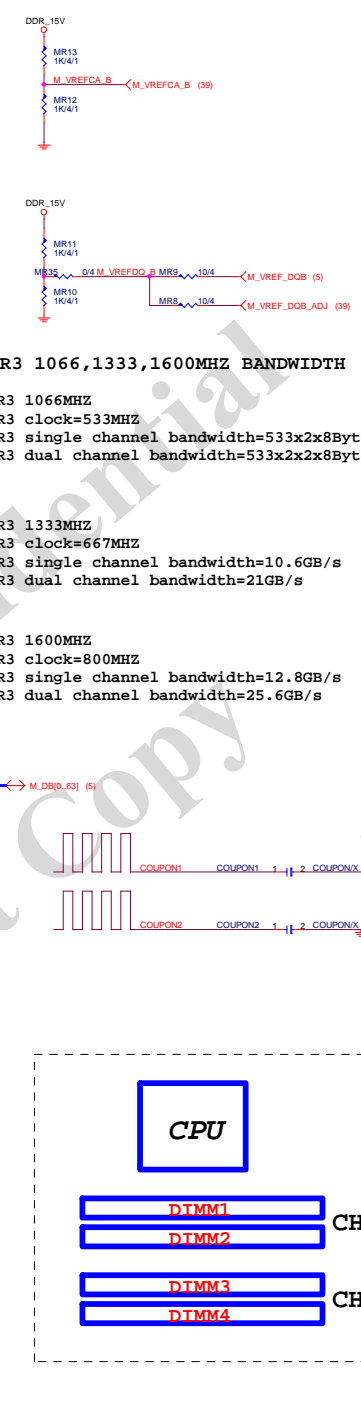




DDR3240/BK/VA/D



DDR3240/BK/VA/D

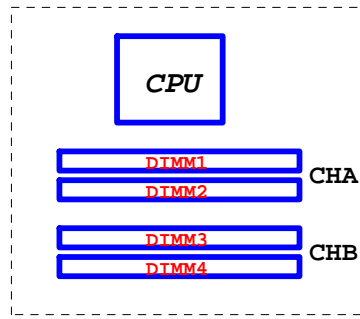
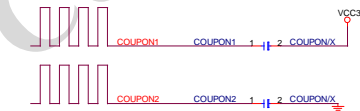


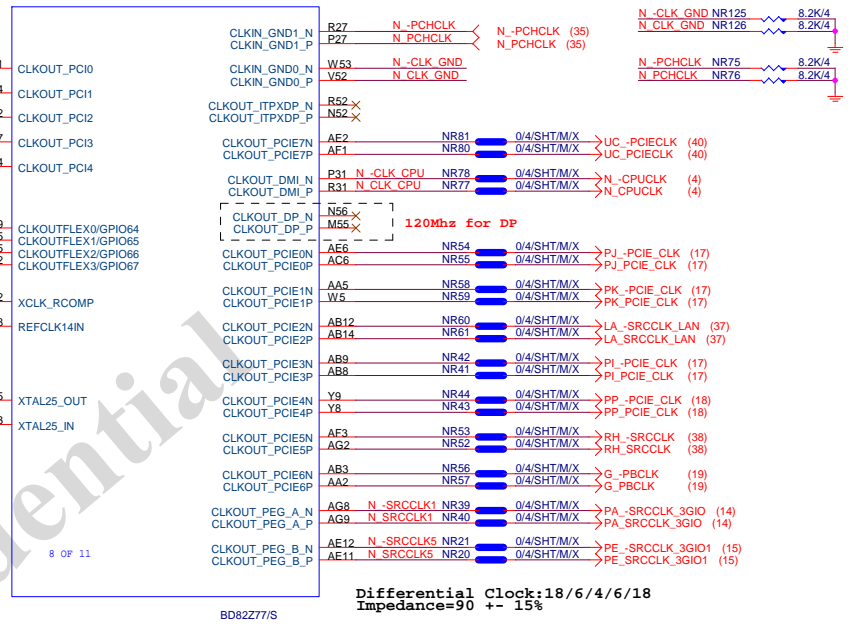
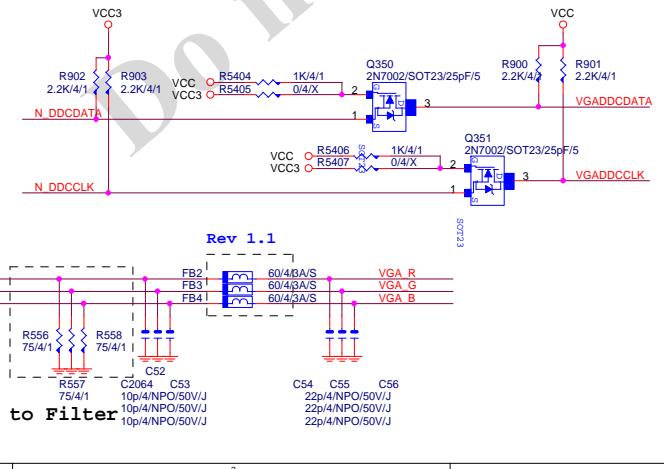
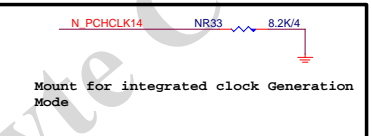
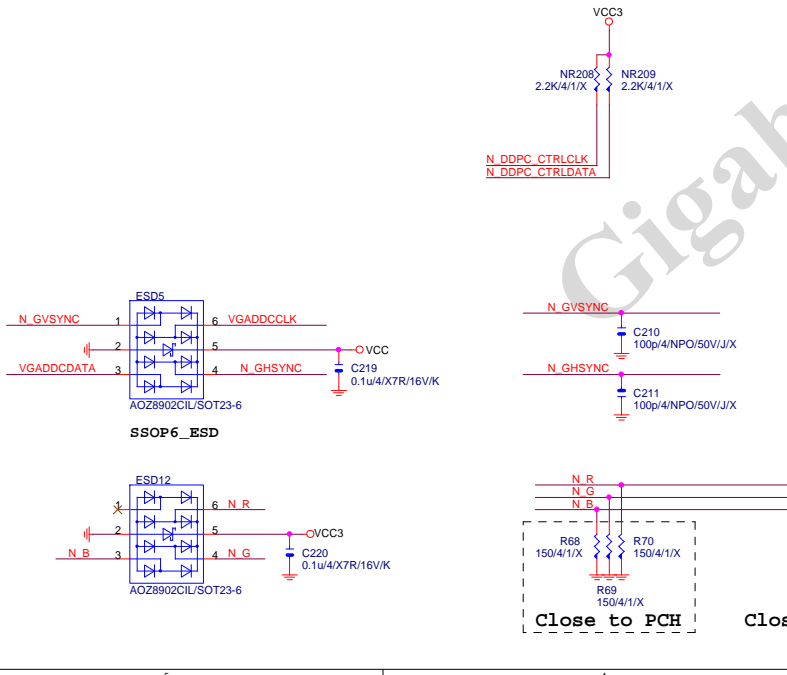
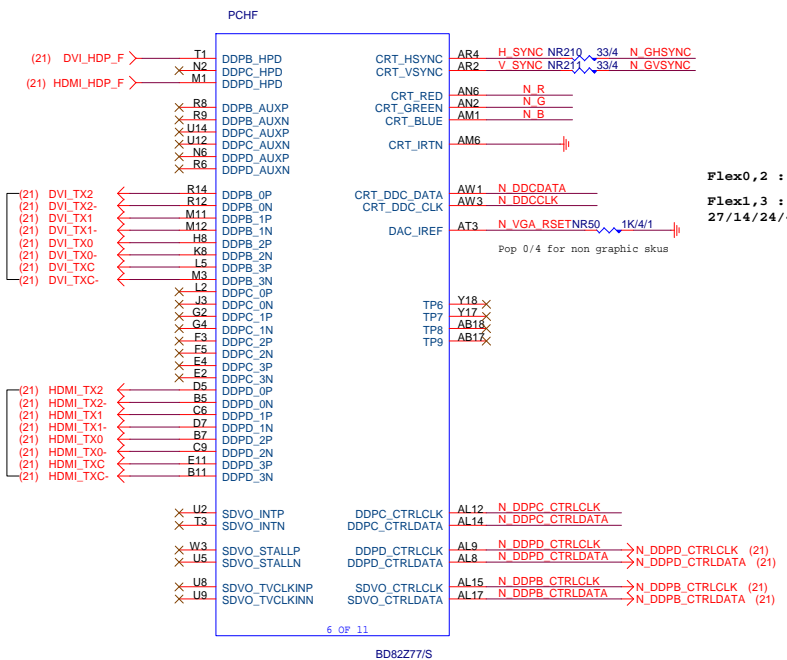
DDR3 1066,1333,1600MHZ BANDWIDTH

DDR3 1066MHZ
DDR3 clock=533MHZ
DDR3 single channel bandwidth=533x2x8Byte=8.5GB/s
DDR3 dual channel bandwidth=533x2x2x8Byte=17GB/s

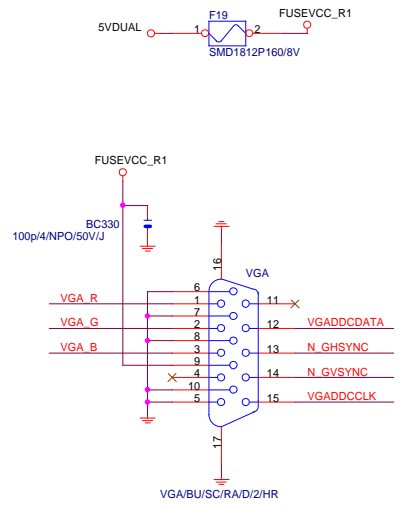
DDR3 1333MHZ
DDR3 clock=667MHZ
DDR3 single channel bandwidth=10.6GB/s
DDR3 dual channel bandwidth=21GB/s

DDR3 1600MHZ
DDR3 clock=800MHZ
DDR3 single channel bandwidth=12.8GB/s
DDR3 dual channel bandwidth=25.6GB/s

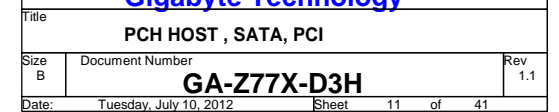


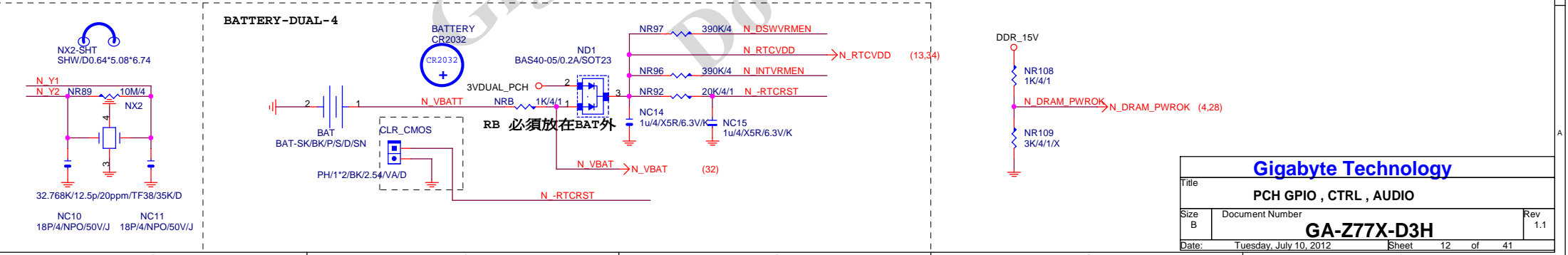
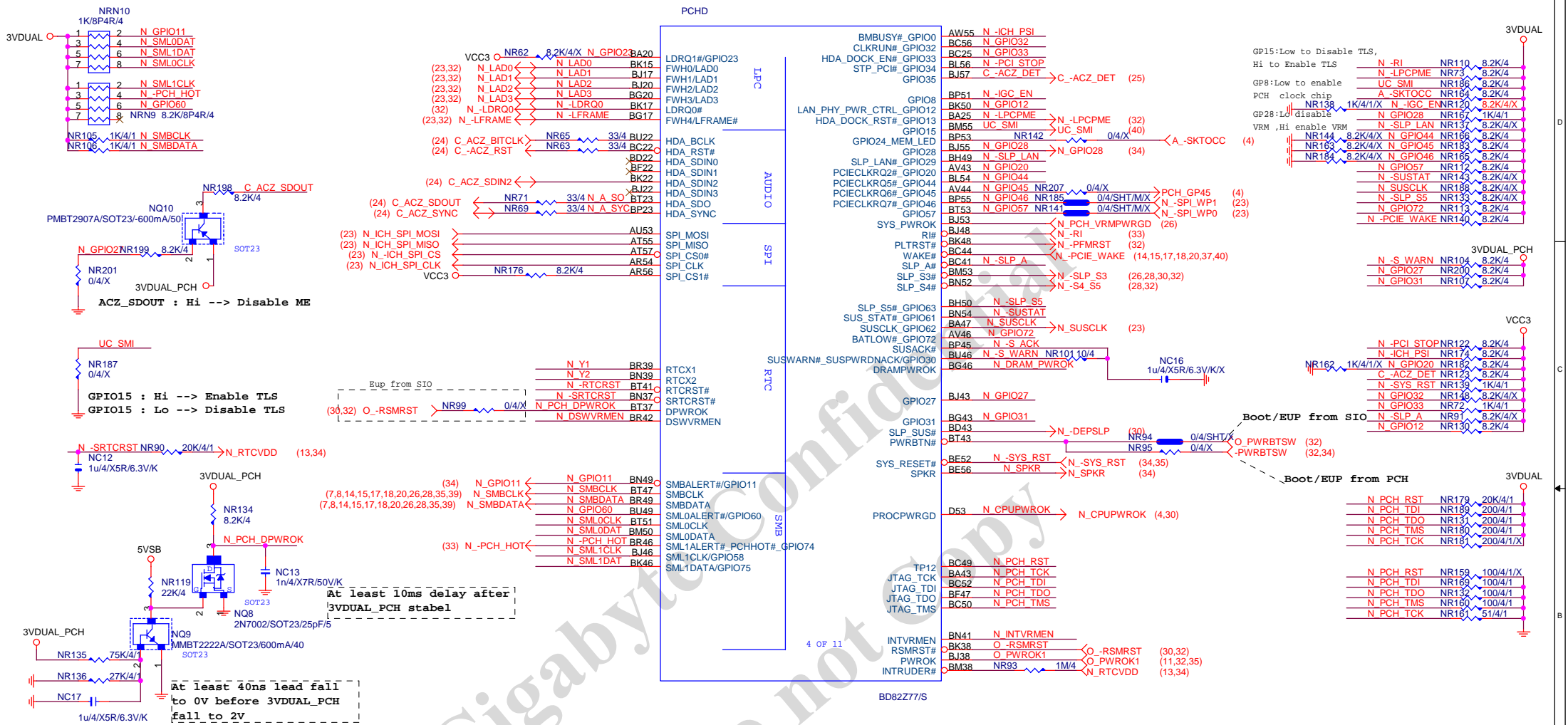


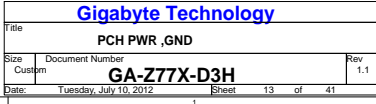
Differential Clock:18/6/4/6/18
Impedance=90 +- 15%

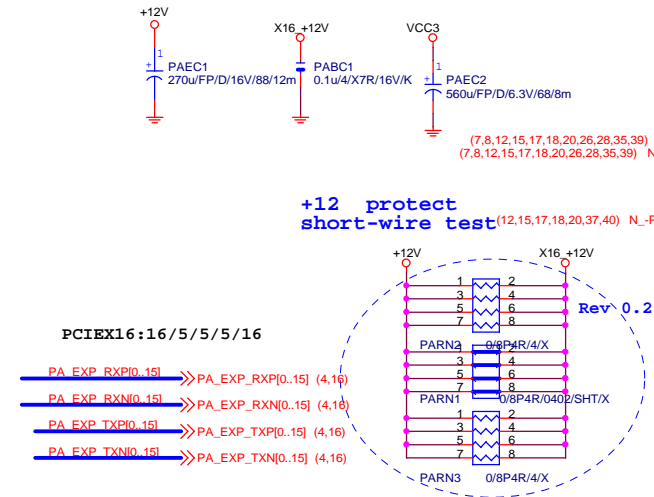


PCHC









PA EXP TXP0	PAC5	0.22u/4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u/4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u/4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u/4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u/4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u/4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u/4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u/4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u/4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u/4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u/4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u/4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u/4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u/4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC19	0.22u/4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC18	0.22u/4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP SW TXP8	PAC20	0.22u/4/X5R/6.3V/K	PA EXP SW TXP8 C
PA EXP SW TXN8	PAC21	0.22u/4/X5R/6.3V/K	PA EXP SW TXN8 C
PA EXP SW TXP9	PAC22	0.22u/4/X5R/6.3V/K	PA EXP SW TXP9 C
PA EXP SW TXN9	PAC23	0.22u/4/X5R/6.3V/K	PA EXP SW TXN9 C
PA EXP SW TXP10	PAC24	0.22u/4/X5R/6.3V/K	PA EXP SW TXP10 C
PA EXP SW TXN10	PAC25	0.22u/4/X5R/6.3V/K	PA EXP SW TXN10 C
PA EXP SW TXP11	PAC26	0.22u/4/X5R/6.3V/K	PA EXP SW TXP11 C
PA EXP SW TXN11	PAC27	0.22u/4/X5R/6.3V/K	PA EXP SW TXN11 C
PA EXP SW TXP12	PAC28	0.22u/4/X5R/6.3V/K	PA EXP SW TXP12 C
PA EXP SW TXN12	PAC29	0.22u/4/X5R/6.3V/K	PA EXP SW TXN12 C
PA EXP SW TXP13	PAC30	0.22u/4/X5R/6.3V/K	PA EXP SW TXP13 C
PA EXP SW TXN13	PAC31	0.22u/4/X5R/6.3V/K	PA EXP SW TXN13 C
PA EXP SW TXP14	PAC32	0.22u/4/X5R/6.3V/K	PA EXP SW TXP14 C
PA EXP SW TXN14	PAC33	0.22u/4/X5R/6.3V/K	PA EXP SW TXN14 C
PA EXP SW TXP15	PAC34	0.22u/4/X5R/6.3V/K	PA EXP SW TXP15 C
PA EXP SW TXN15	PAC35	0.22u/4/X5R/6.3V/K	PA EXP SW TXN15 C

PA EXP SW RXP8.15	>>>PA_EXP_SW_RXP8.15	(16)
PA EXP SW RXN8.15	>>>PA_EXP_SW_RXN8.15	(16)
PA EXP SW TXP8.15	>>>PA_EXP_SW_TXP8.15	(16)
PA EXP SW TXN8.15	>>>PA_EXP_SW_TXN8.15	(16)

PCI-E REV:1.1--> 2.5GHZ

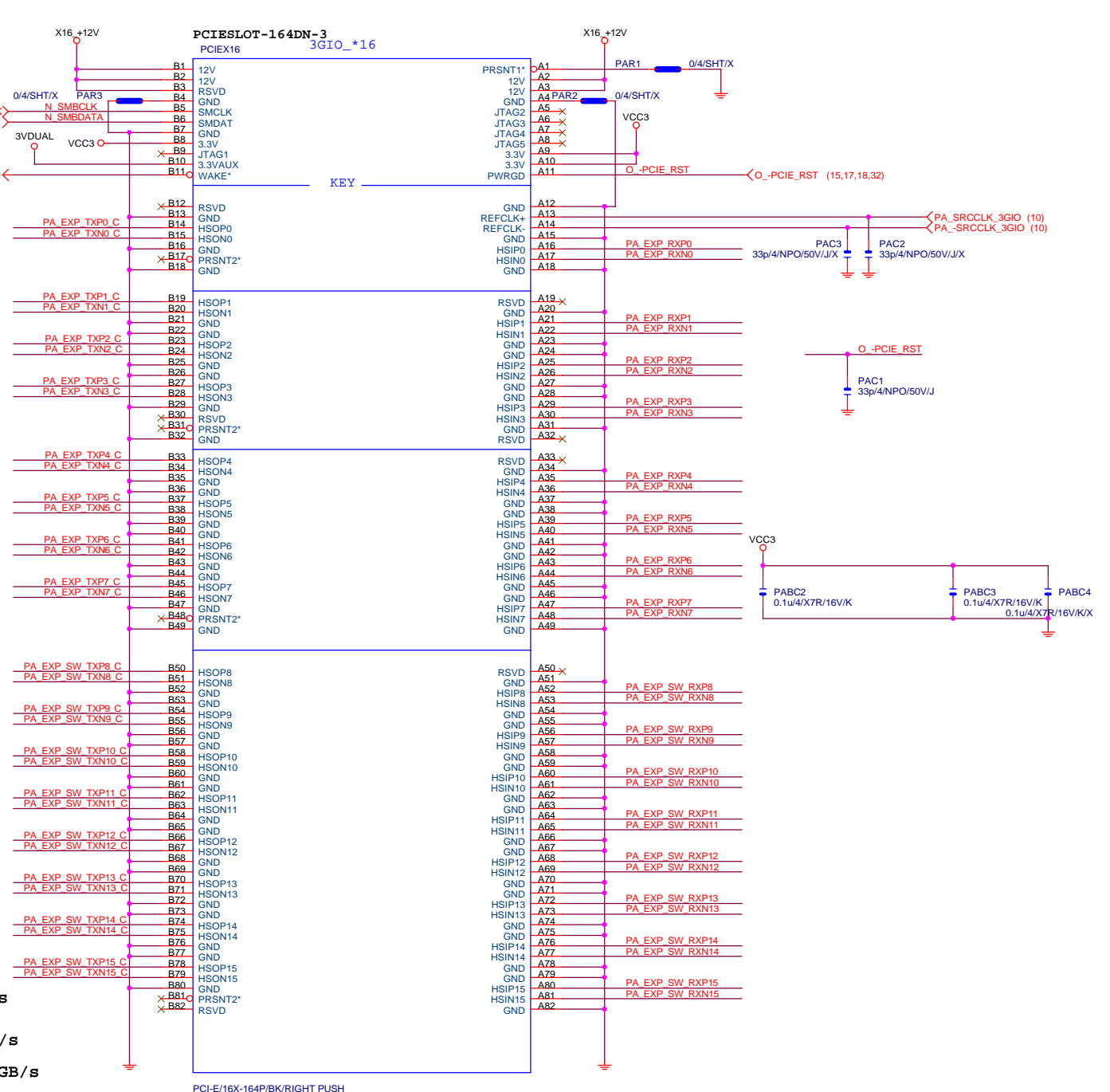
PCE-E X1(單向) BANDWITH=2.5GHz*(8b/10b)=2Gb/s=250MB/s

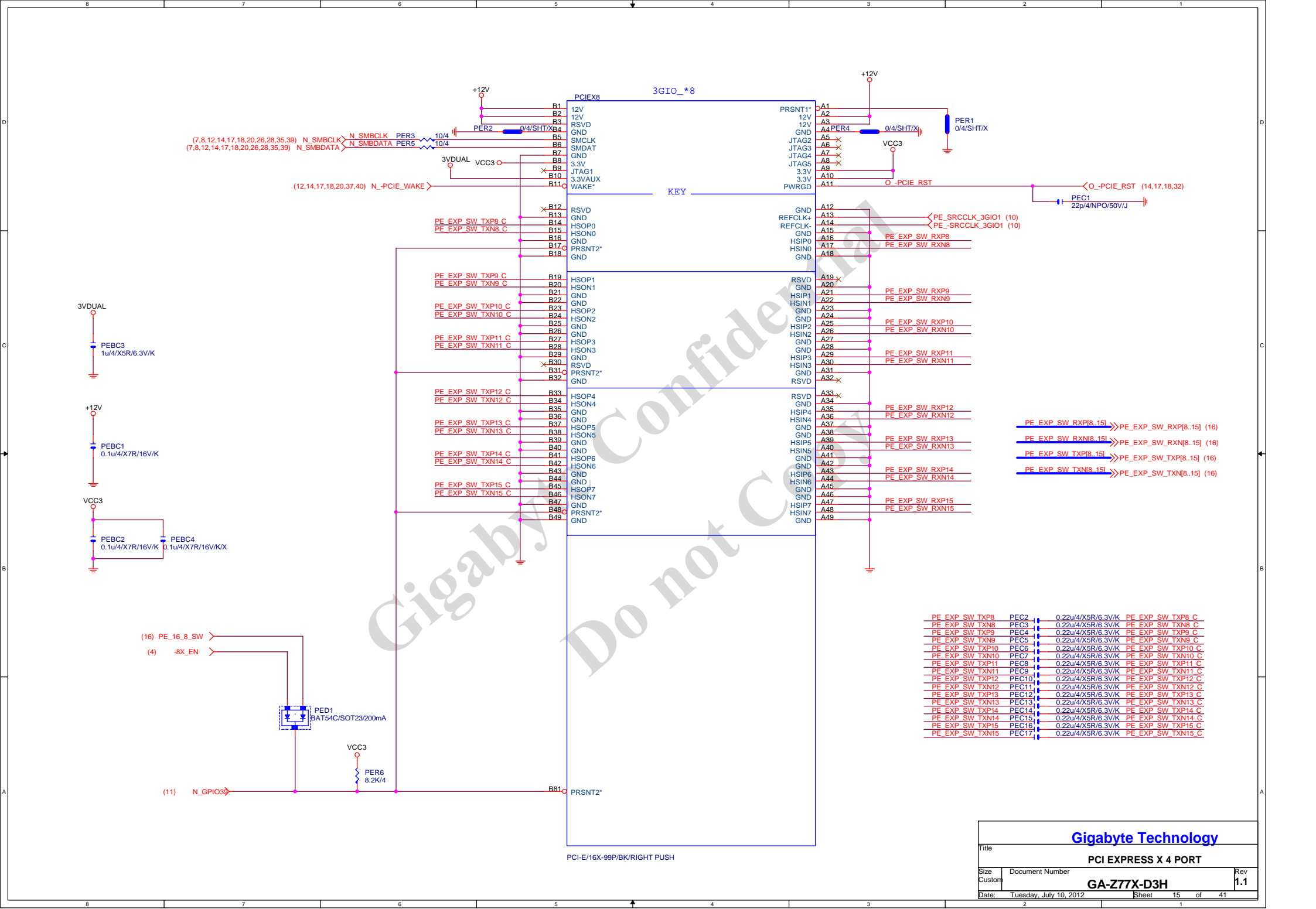
PCE-E X1(雙向) BANDWITH=2.5GHz*(8b/10b)X2=4Gb/s=500MB/s

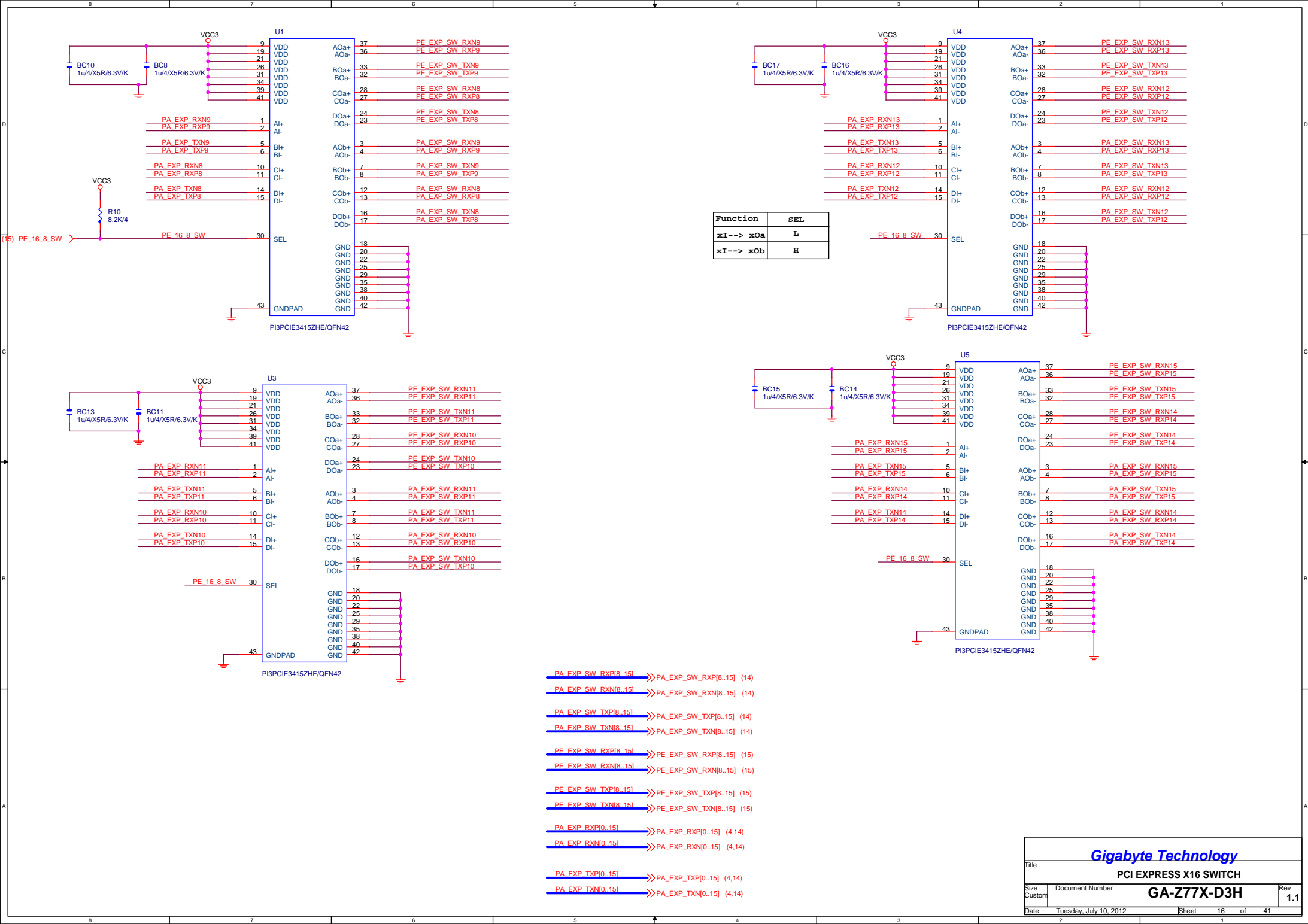
PCE-E X16(單向) BANDWITH=2.5GHz*(8b/10b)X16=32Gb/s=4GB/s

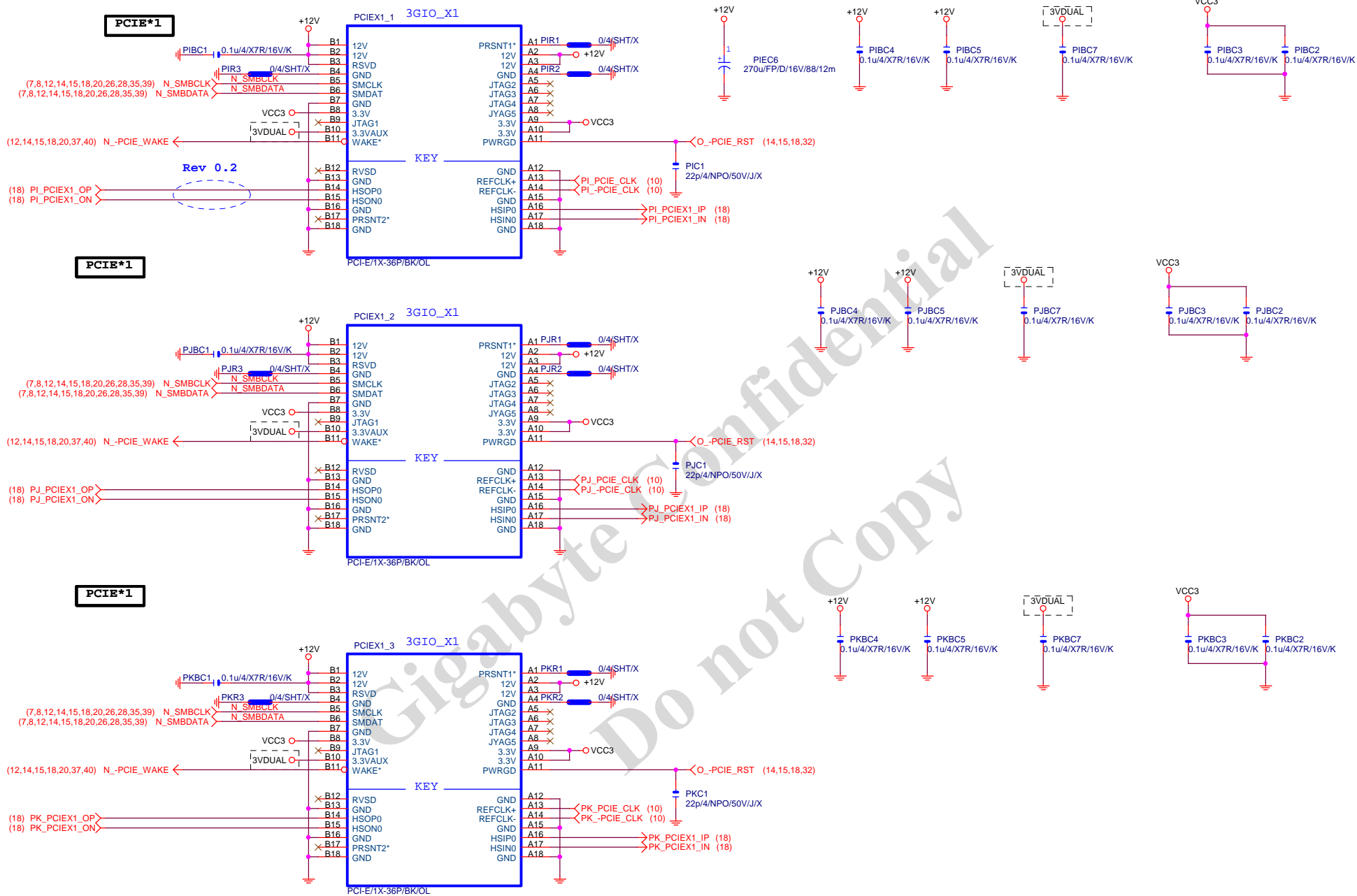
PCE-E X16(雙向) BANDWITH=2.5GHz*(8b/10b)X16X2=64Gb/s=8GB/s

PCI-E REV:2.0--> 5GHZ



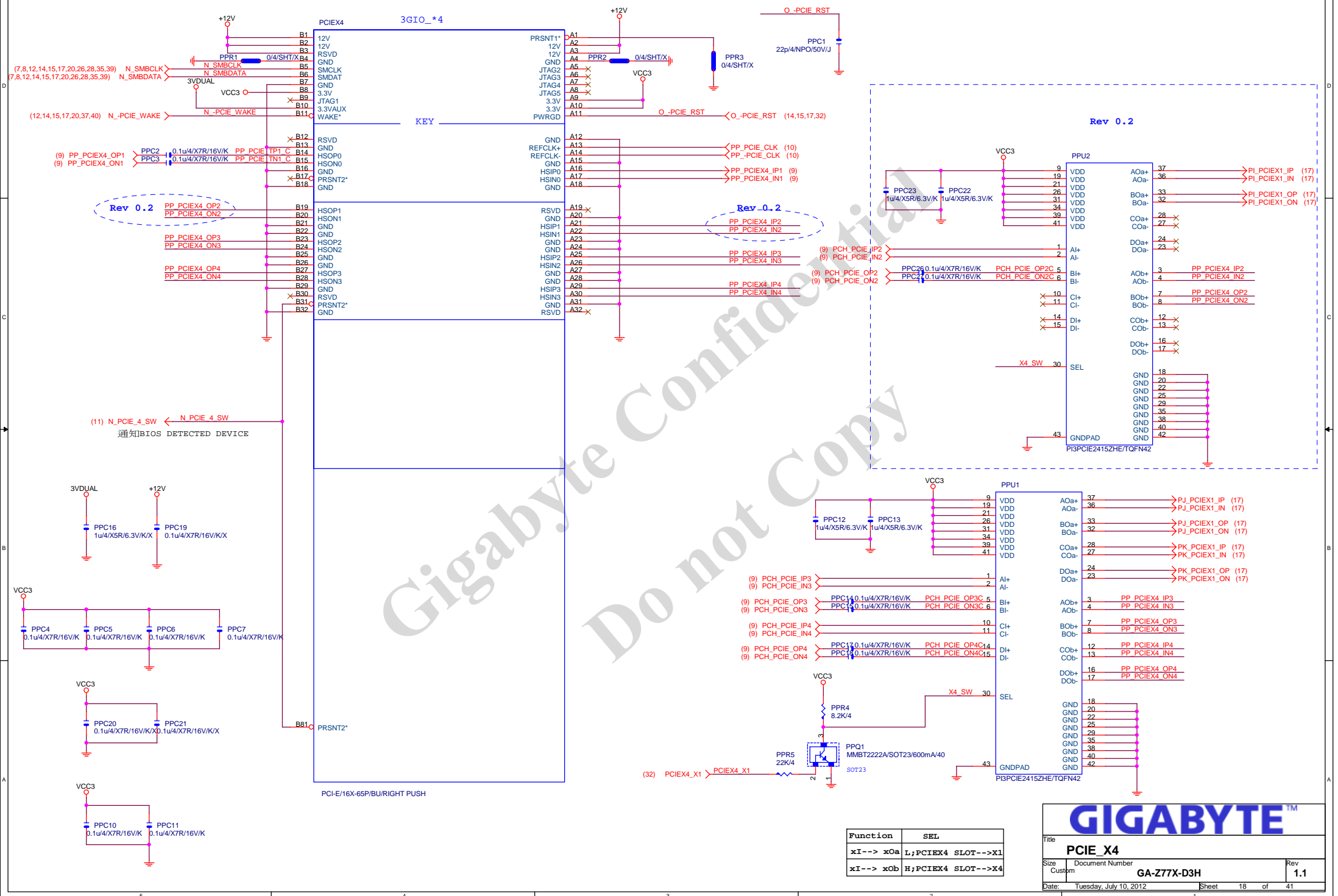




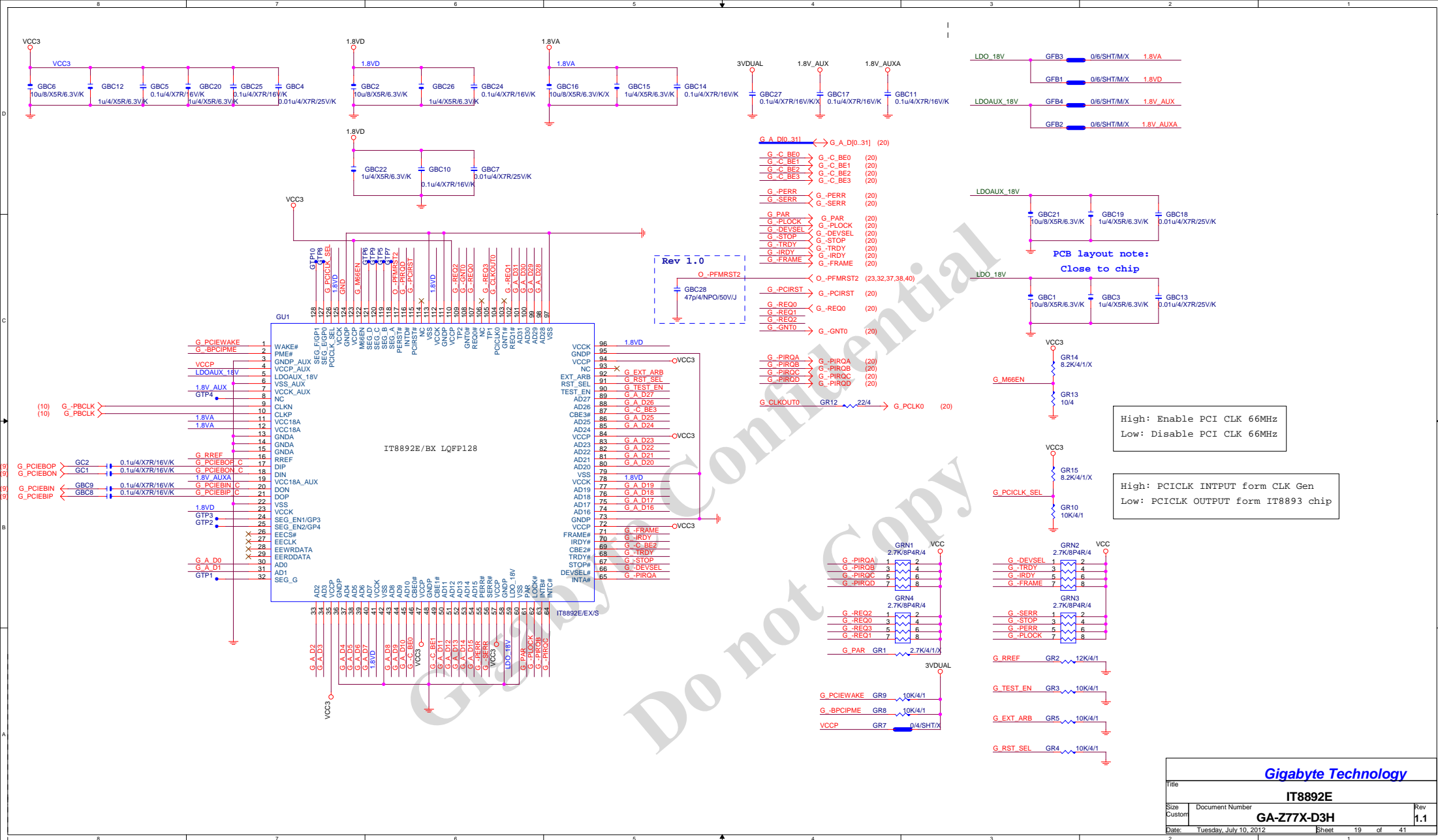


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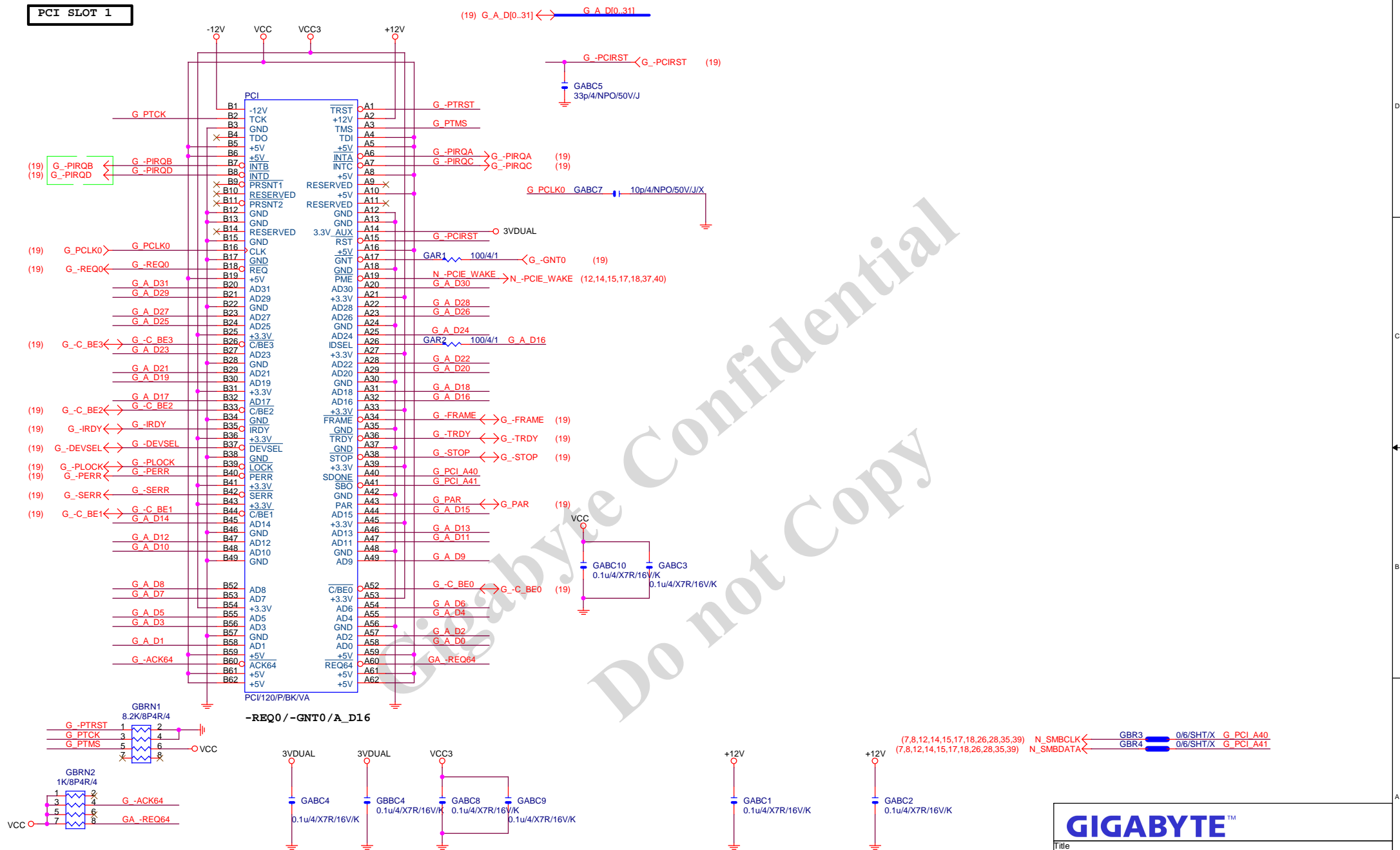
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Size	Document Number		Rev	
Custom	GA-Z77X-D3H		1.1	
Date:	Tuesday, July 10, 2012	Sheet	17	of 41



Function	SEL
xI--> x0a	L;PCIEX4 SLOT-->
xI--> x0b	H;PCIEX4 SLOT-->

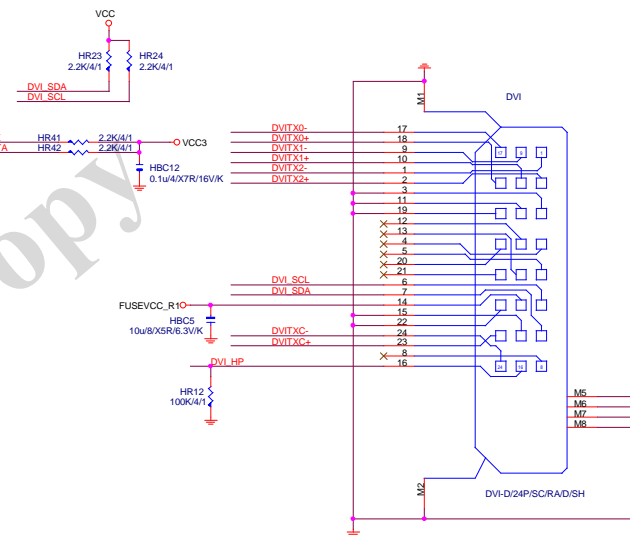
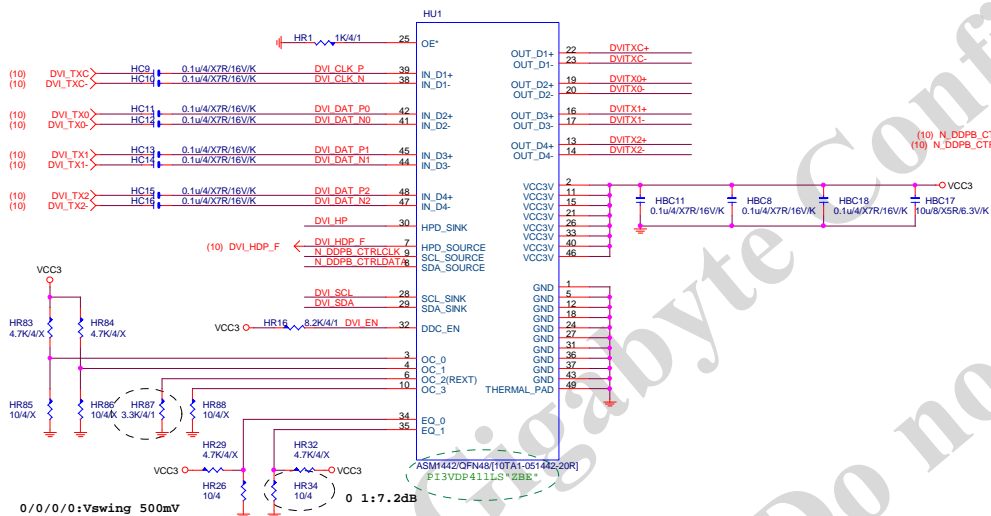
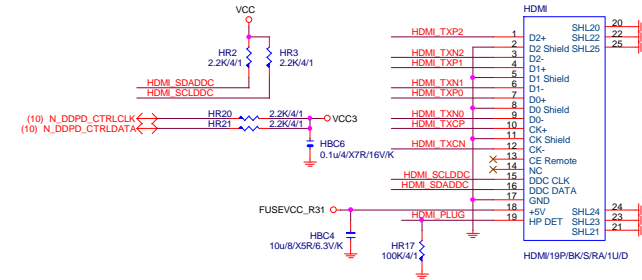
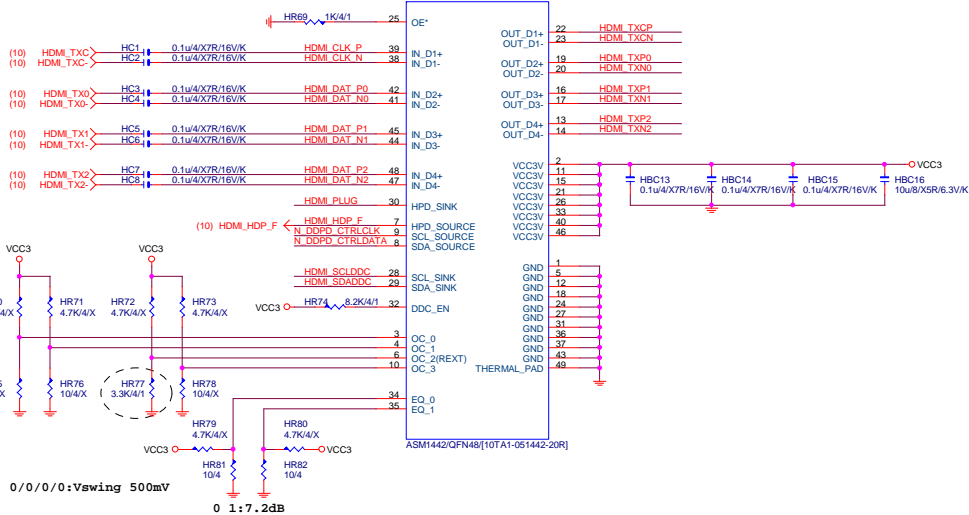


PCI SLOT 1

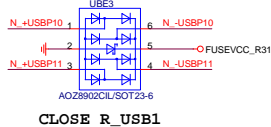
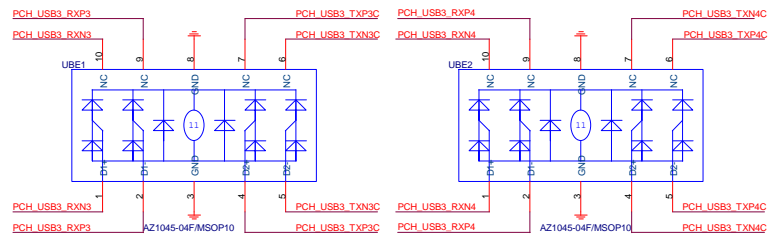


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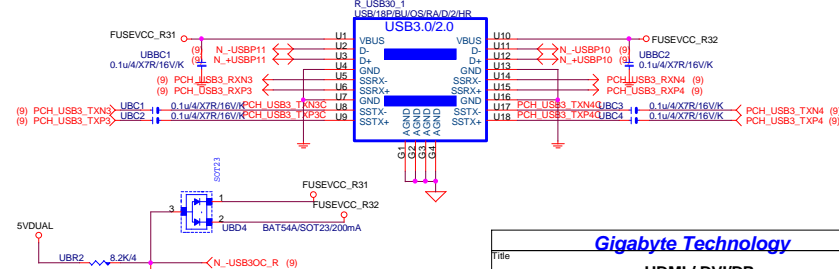
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PCI SLOT 1&2			
Size	Document Number	Rev	
Custom	GA-Z77X-D3H	1.1	
Date:	Tuesday, July 10, 2012	Sheet	20 of 41



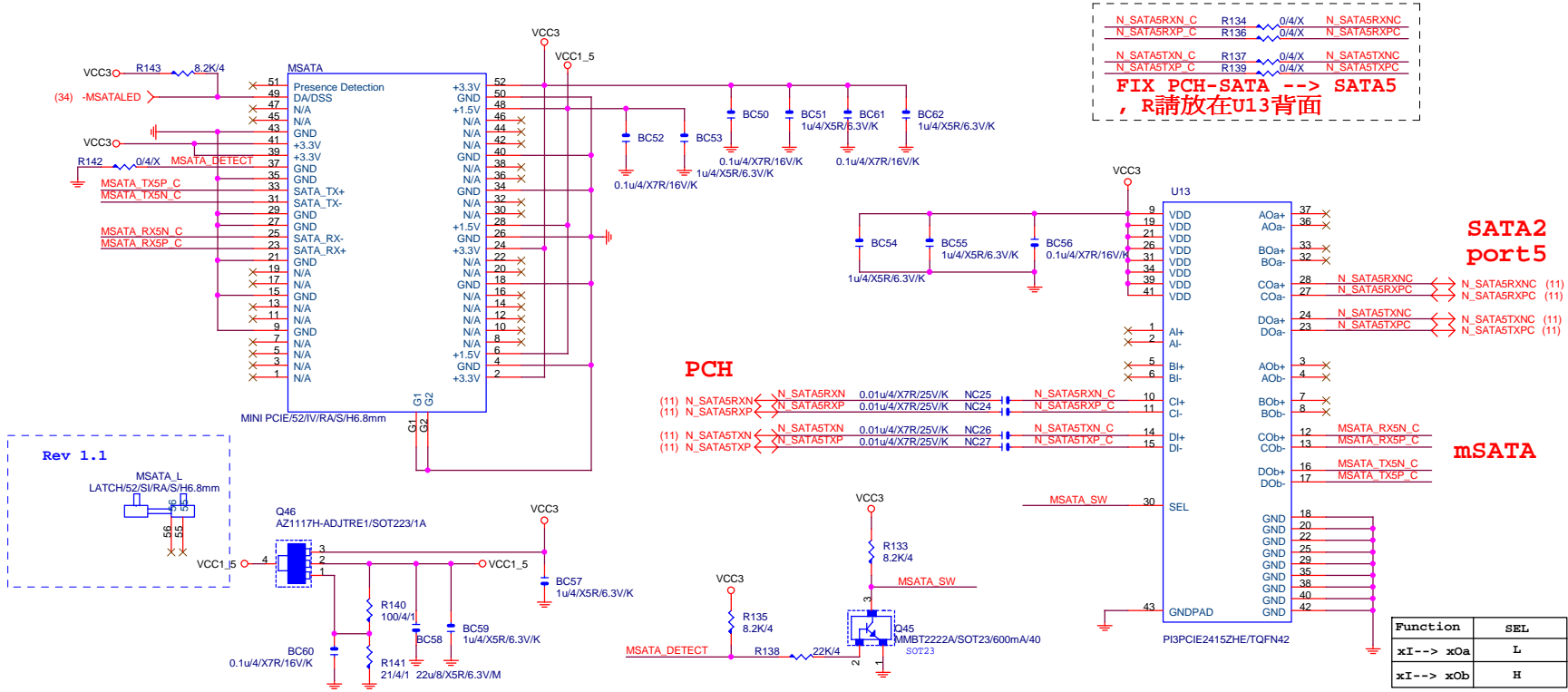
USB3.0



USB30_20



Gigabyte Technology			
HDMI / DVI/DP			
GA-Z77X-D3H			
Rev	1.1		
Date:	Tuesday, July 10, 2012	Sheet	21 of 41



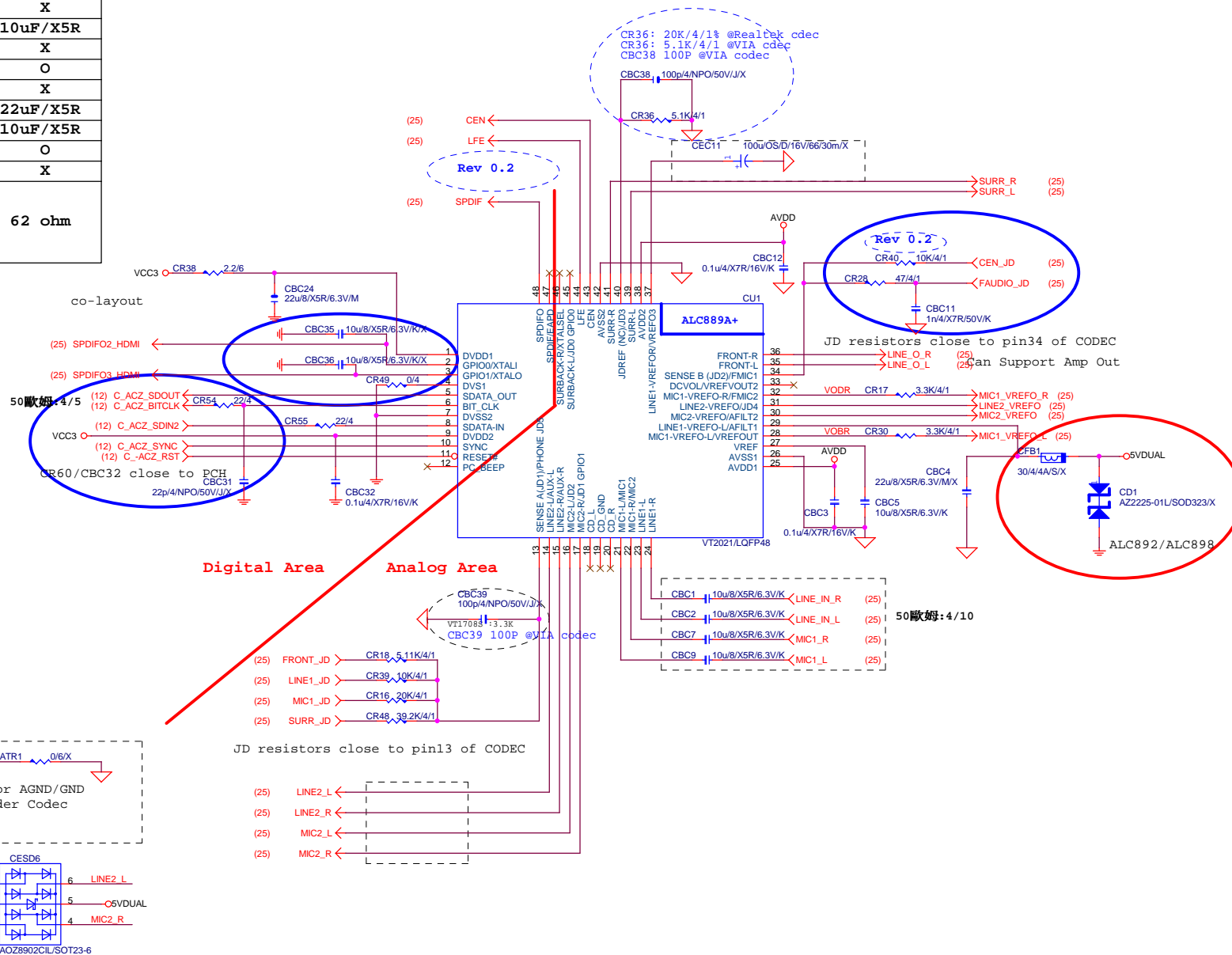
FIX PCH-SATA --> SATA5
R請放在U13背面

SATA2
port5

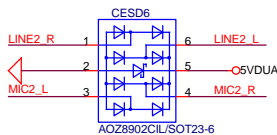
mSATA

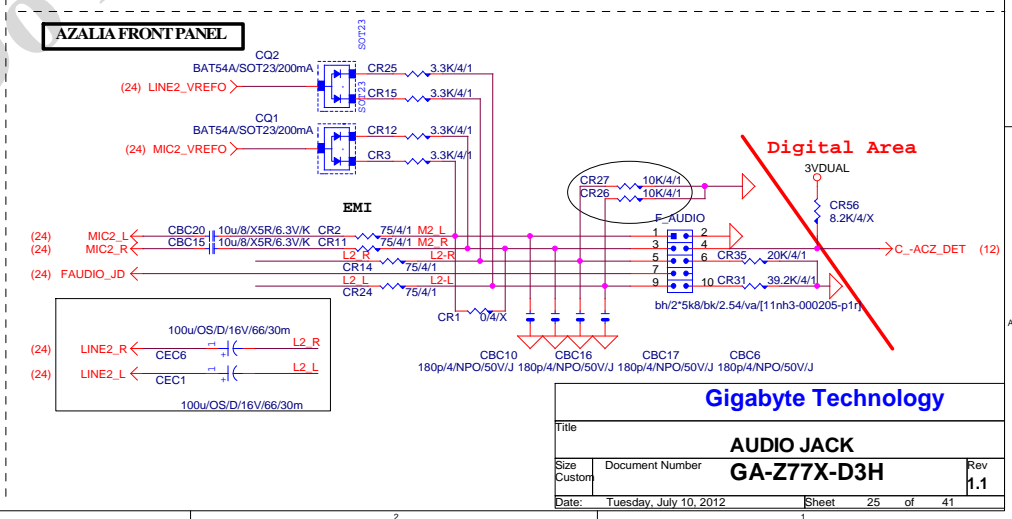
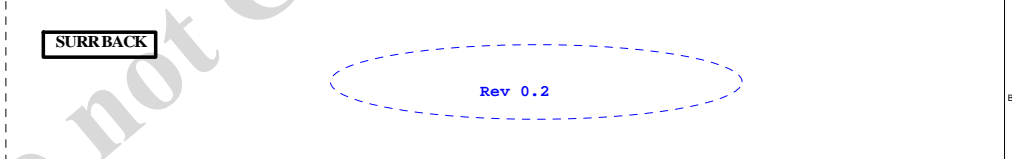
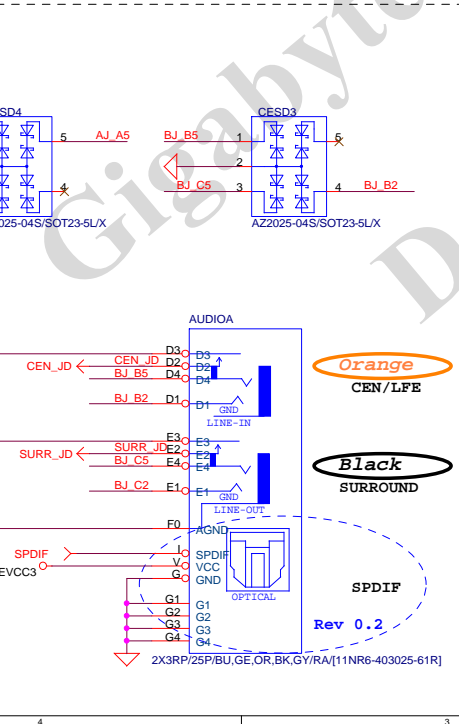
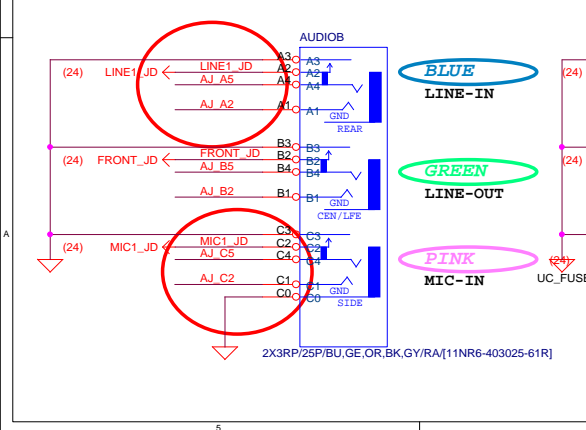
Function	SEL
xI--> xOa	L
xI--> xOb	H

	ALC889	ALC889B	ALC898/ALC892
CR49	O	O	X
CBC36	X	X	10uF/X5R
CBC35	X	10uF/X5R	X
CR52	O	X	O
CR53	X	O	X
CBC1/CBC2	22uF/X5R	22uF/X5R	22uF/X5R
CBC7/CBC9/CBC20/CBC15	10uF/X5R	10uF/X5R	10uF/X5R
CFB1/CD1/CBC4	X	X	O
CD2/CD3/CQ3/CQ4	O	O	X
CR7/CR9/CR5/CR13/ CR29/CR32/CR46/CR19/ CR50/CR41/CR21/CR47/ CR2/CR11/CR14/CR24	62 ohm	62 ohm	62 ohm

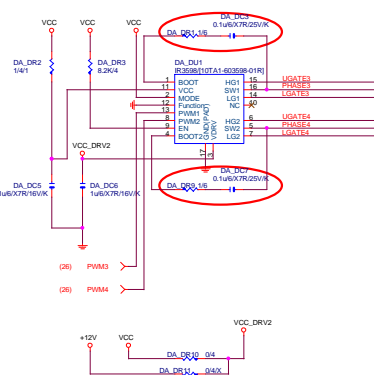


SMOATR1 0/6/X For AGND/GND moat under Codec Body





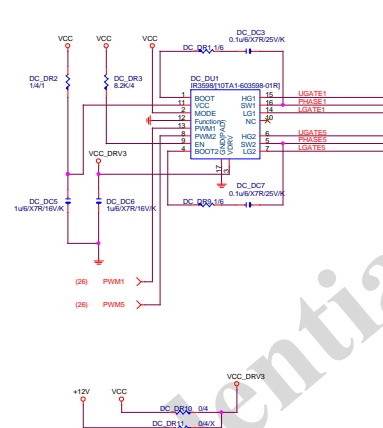
VCORE Phase 3,6



FUNCTION	MODE	PMN MODE	PHASE MODE
0	1	1R ATL	DUAL
1	1	1R ATL	Doubler
0	0	Tri-Seats	DUAL
1	0	Tri-Seats	Doubler
OPEN	0	Tri-Seats	Quad
OPEN	1	1R ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin9 link to IC2 pin9 without PU

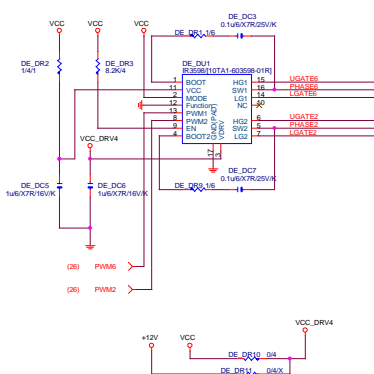
VCORE Phase 1,4



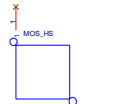
FUNCTION	MODE	PWM MODE	PHASE MODE
0	1	1R ATL	DGAL
1	1	1R ATL	Doubler
0	0	Tri-Saats	DGAL
1	0	Tri-Saats	Doubler
OPEN	0	Tri-Saats	Quad
OPEN	1	1R ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
IC1 pin8 link to IC2 pin8 without SW

VCORE Phase 5,2

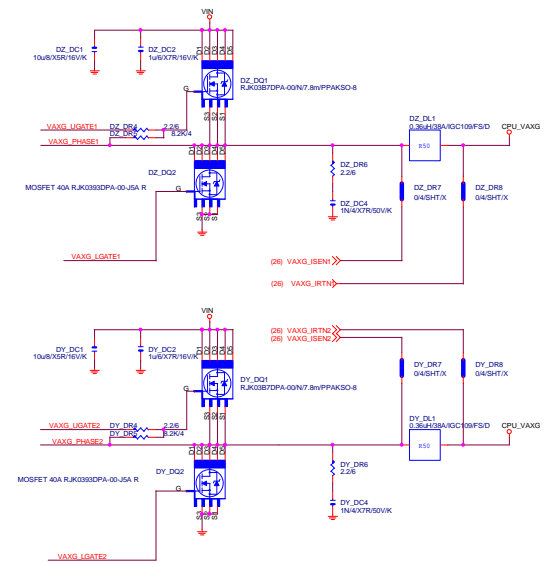
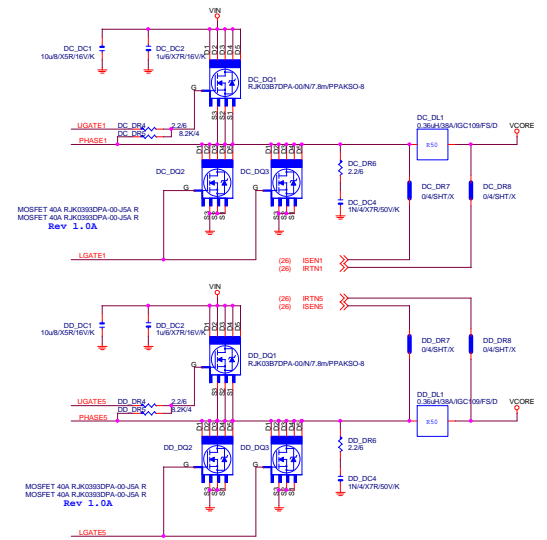
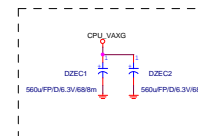
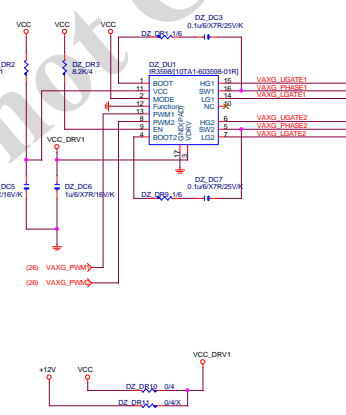


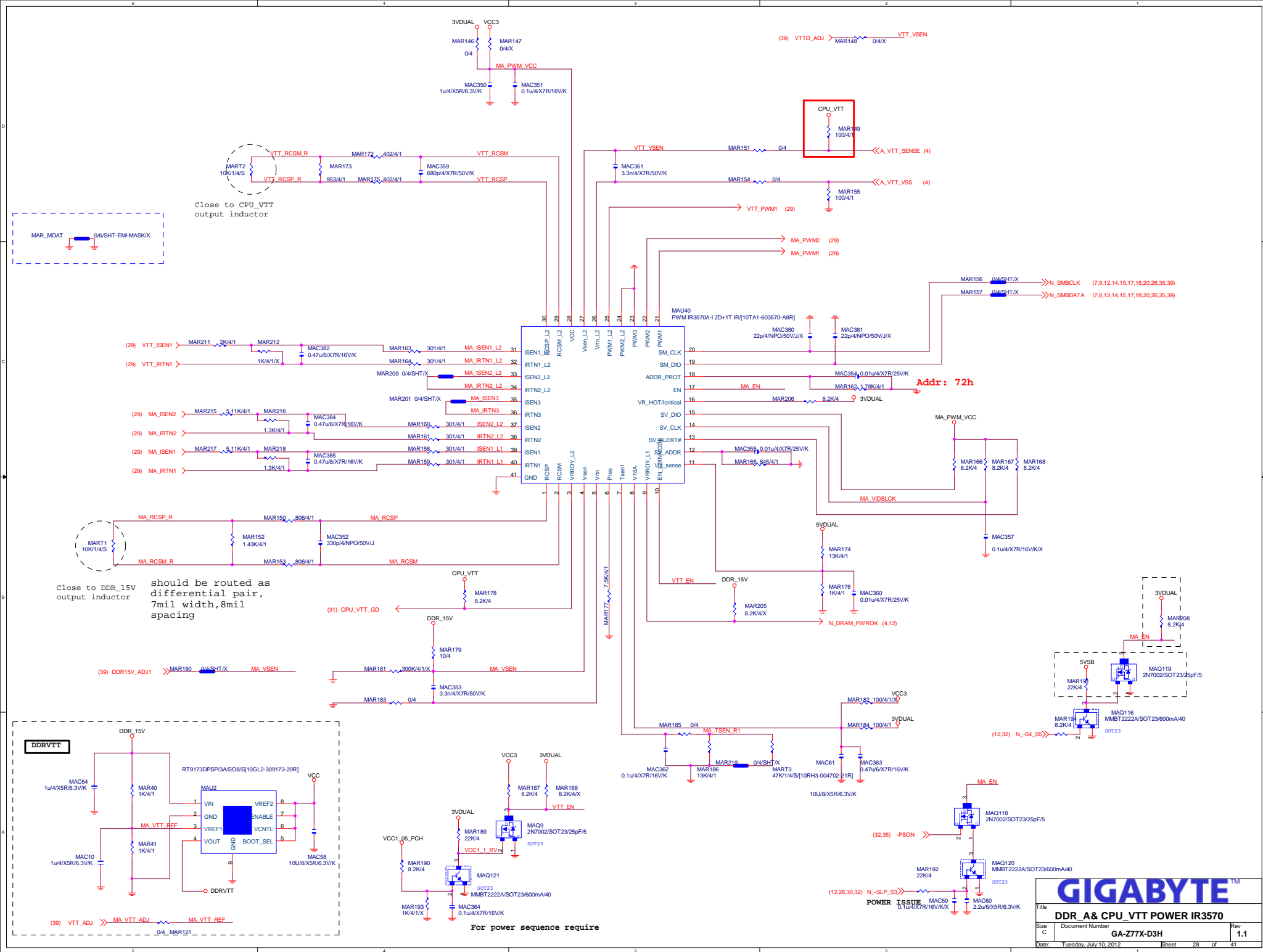
MOS HEATSINK



MOS HS[12SP2-S08924-01R_12SP2-S08924-02R_12SP2-S08924-03R]

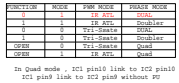
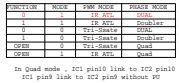
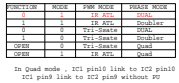
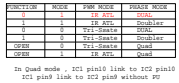
VAXG Phase

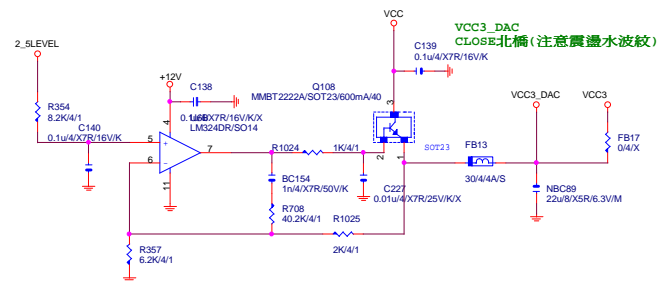
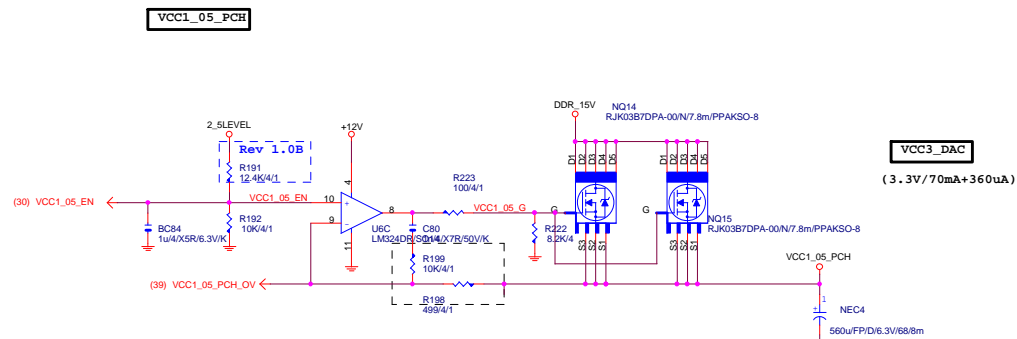




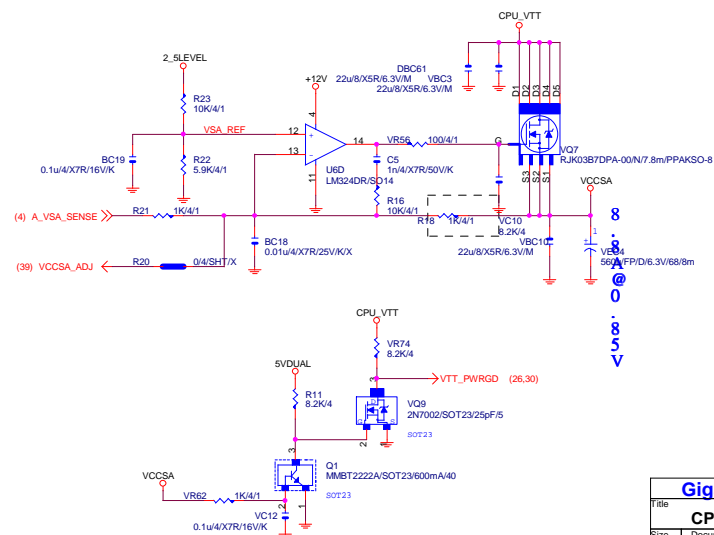
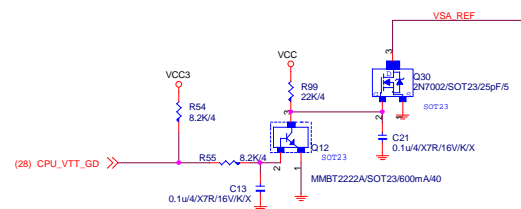
FUNCTION	MODE	PMW MODE	PHASE MODE
0	1	IR ATL	DUAL
1	1	IR ATL	Doubler
0	0	Tri-Saats	DUAL
1	0	Tri-Saats	Doubler
OPEN	0	Tri-Saats	Quad
OPEN	1	IR ATL	Quad

In Quad mode , IC1 pin10 link to IC2 pin10
 IC1 pin9 link to IC2 pin9 without PG

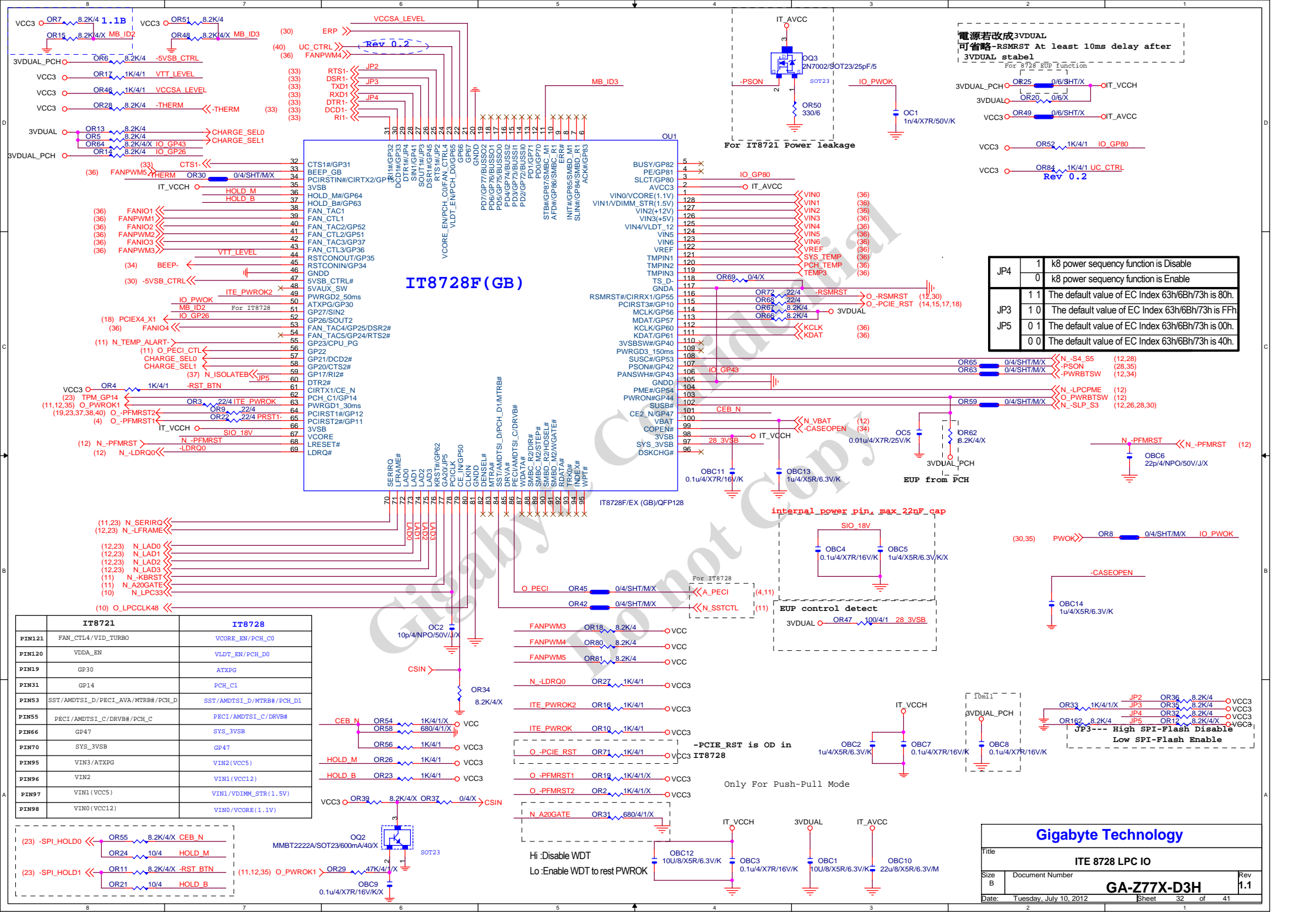


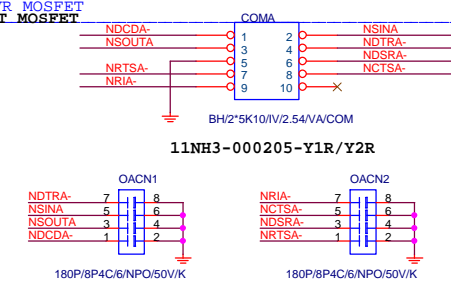
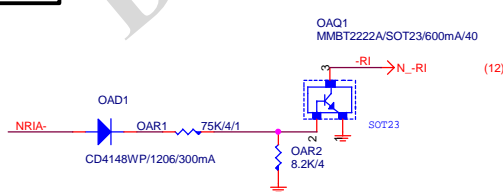
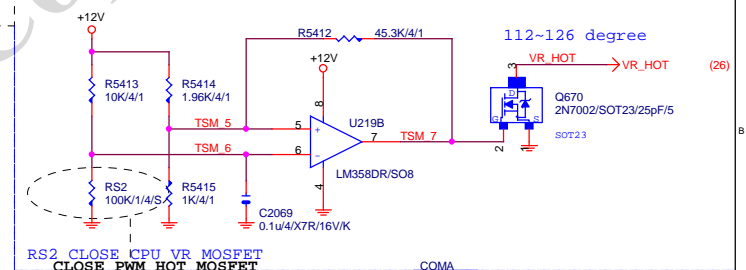
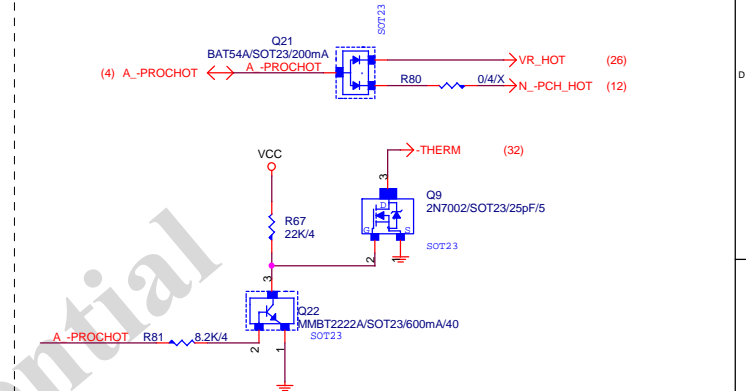


VCC_SA

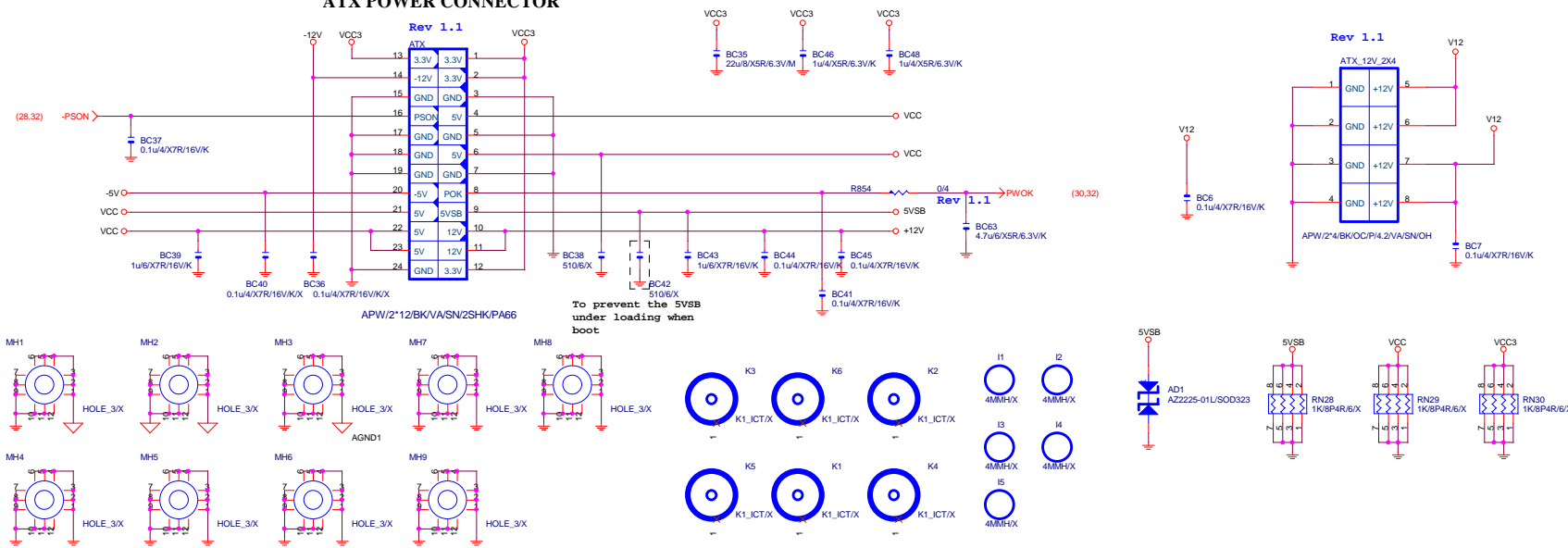


Gigabyte Technology			
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C		Rev	1.1
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ATX POWER CONNECTOR



CLK GEN CK505

CPU Frequency Selection

FSLB	FSLA	CPU
0	0	100M <Default>
0	1	133M
1	0	200M
1	1	166M

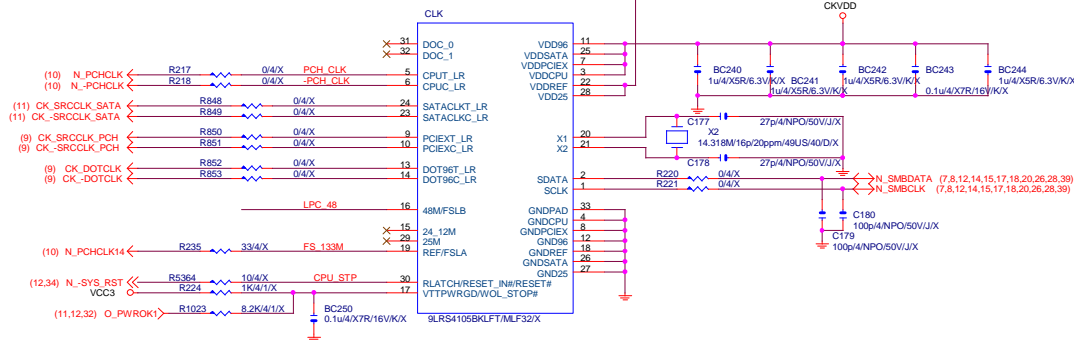
N_PCHCLK14 C182 10p/4/NPO/50V/J/X

CKVDD R241 8.2K/4/1/X FS_133M

CKVDD R237 8.2K/4/1/X CPU_STP

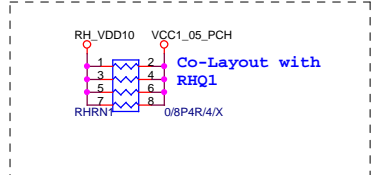
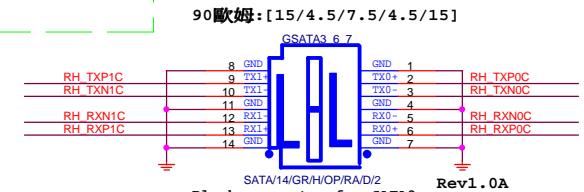
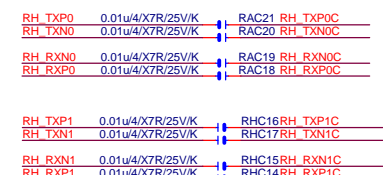
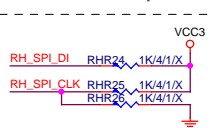
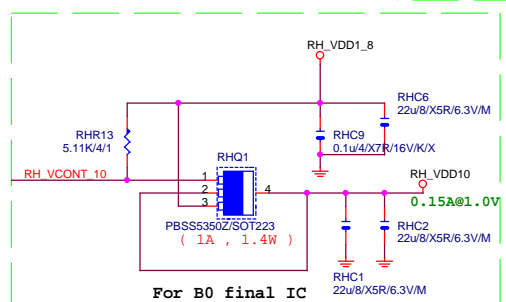
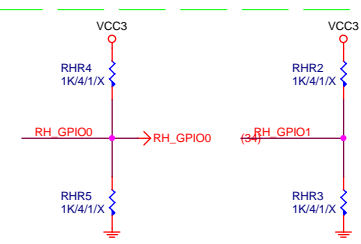
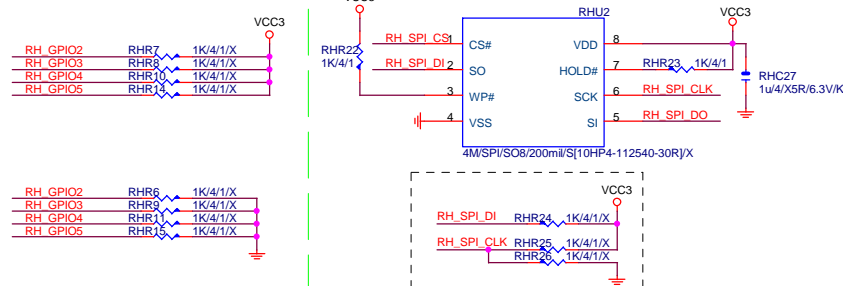
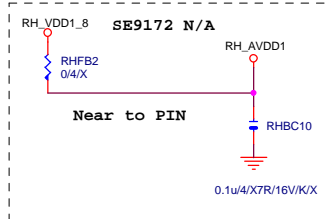
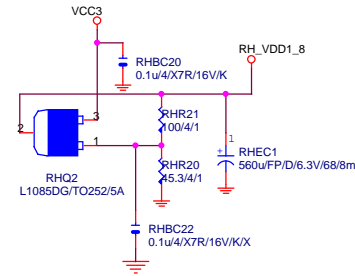
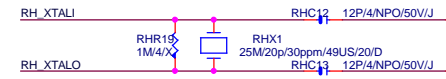
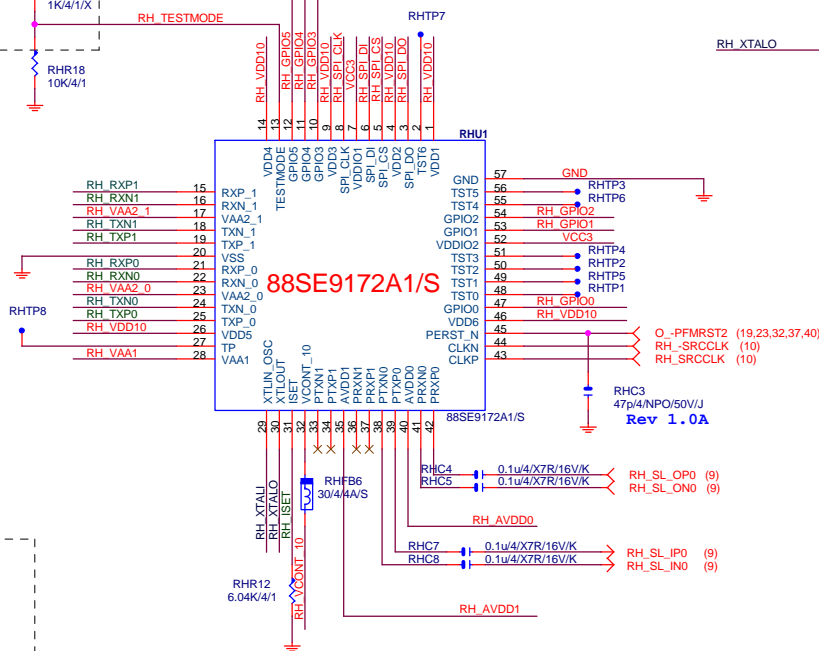
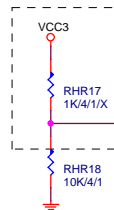
CKVDD R5384 8.2K/4/1/X

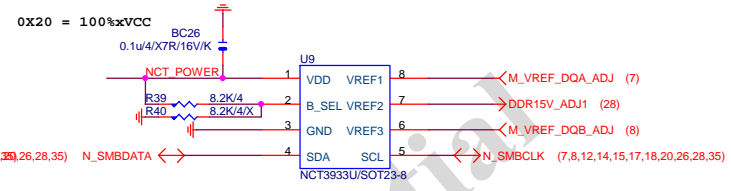
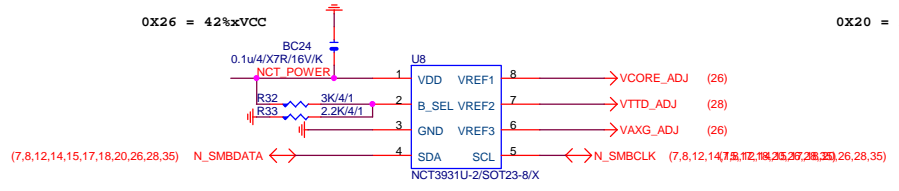
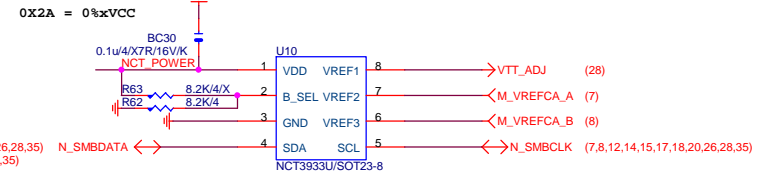
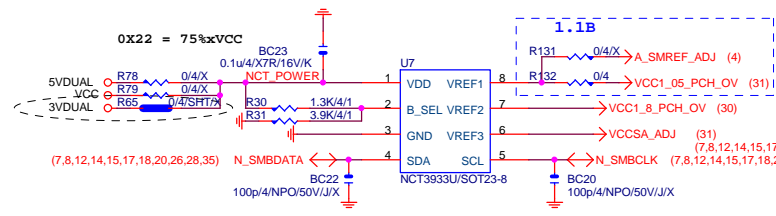
R992 8.2K/4/1 LPC_48



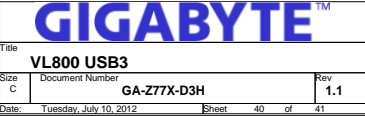
Gigabyte Technology

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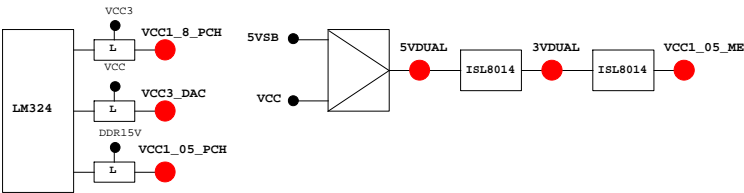


PCH GPIO LIST TABLE					
PIN NAME	PWR	Default	USAGE	NOTE	
GP0	MAIN	H-Z	GPI -PECI_REQ	N/A	
GP1/TACH1	MAIN		GPI ICH_FAN_TACH1	N/A	
GP2/PIRQ#	MAIN		GPI -PIRQE	P/U 8.2K VCC3	
GP3/PIRQ#	MAIN		GPI -PIRQF	P/U 8.2K VCC3	
GP4/PIRQG#	MAIN		GPI -PIRQG	P/U 8.2K VCC3	
GP5/PIRQH#	MAIN		GPI -PIRQH	P/U 8.2K VCC3	
GP6/TACH2	MAIN		GPI ICH_FAN_TACH2	N/A	
GP7/TACH3	MAIN		GPI ICH_FAN_TACH3	N/A	
GP8	STBY	H	GPO GPIO8	P/U 8.2K 3VDUAL	
GP9/OC5#	STBY		NATIVE OC5#	N/A	
GP10/OC6#	STBY		NATIVE OC6#	N/A	
GP11/SMBALERT#	STBY		NATIVE -SMBALERT	P/U 8.2K 3VDUAL	
GP12	STBY	L	GPI LAN_PHY_PWR_CTRL	P/U 8.2K 3VDUAL	
GP13	STBY	L	GPI GPIO13	P/U 8.2K 3VDUAL	
GP14/OC7#	STBY		NATIVE OC7#	N/A	
GP15	STBY	L	GPO GPIO15	N/A	
GP16	MAIN		GPI -SKT0CC	P/U 8.2K VCC3	
GP17/TACH0	MAIN		GPI ICH_FAN_TACH0	N/A	
GP18	MAIN		NATIVE MB_ID0	P/D 8.2K GND	
GP19	MAIN		GPI -LAN1_ISO	P/U 8.2K VCC3	
GP20	MAIN		NATIVE LED_CTL	P/U 1K VCC3	
GP21	MAIN		GPI VCC18_FCH_OV2	P/U 8.2K VCC3	
GP22	MAIN	H-Z	GPI VCORE_OV3	P/U 8.2K VCC3	
GP23	MAIN		NATIVE -LDRQ1	P/U 8.2K VCC3	
GP24	STBY	L	GPO TLS	P/U 8.2K 3VDUAL	
GP25	STBY		NATIVE -CPU_STOP	P/U 8.2K 3VDUAL	
GP26	STBY		NATIVE -ACZ_DET	P/U 8.2K 3VDUAL	
GP27	STBY	H	GPO GPIO27	P/U 8.2K 3VDUAL	
GP28	STBY	H	GPO GPIO28	P/U 8.2K 3VDUAL	
GP29	STBY	L	GPI GPIO29	N/A	
GP30	STBY	H-Z	GPI S_PWR_ACK	P/U 100K 3VDUAL	
GP31	STBY	H-Z	GPI N/A(Reverse)	P/U 8.2K VCC3	
GP32	MAIN	H	GPO MB_ID1	P/D 8.2K GND	
GP33	MAIN	H	GPO LOAD-LINE	P/U 1K VCC3	
GP34	MAIN	H-Z	GPI -PCI_STOP	P/U 8.2K VCC3	
GP35	MAIN	L	GPO GPIO35	P/U 8.2K VCC3	
GP36	MAIN		GPI -LAN1_DSM	P/U 8.2K VCC3	
GP37	MAIN		GPI N/A	P/U 8.2K VCC3	
GP38	MAIN	H-Z	GPI VCORE_OV2	P/U 8.2K VCC3	
GP39	MAIN	H-Z	GPI -LAN_DSM	P/U 8.2K VCC3	
GP40	STBY		NATIVE OC1#	N/A	
GP41	STBY		NATIVE OC2#	N/A	
GP42	STBY		NATIVE OC3#	N/A	
GP43	STBY		NATIVE OC4#	N/A	
GP44	STBY	L	NATIVE N/A	P/U 8.2K 3VDUAL	
GP45	STBY		NATIVE -LPCPME	P/U 8.2K 3VDUAL	
GP46	STBY	L	NATIVE PWR_LED	P/U 8.2K 3VDUAL	
GP47	STBY		NATIVE PSI_LED	P/U 8.2K 3VDUAL	
GP48	MAIN	H-Z	IN EN_PWM	P/U 8.2K VCC3	
GP49	MAIN	H-Z	IN VCC18_OV1	P/U 8.2K VCC3	
GP50	MAIN		NATIVE -REQ1	P/U 2.2K VCC	
GP51	MAIN	H	NATIVE -GNT1	N/A	
GP52	MAIN		NATIVE -REQ2	P/U 2.2K VCC	
GP53	MAIN	H	NATIVE -GNT2	N/A	
GP54	MAIN		NATIVE -REQ3	P/U 2.2K VCC	
GP55	MAIN	H	NATIVE -GNT3	N/A	
GP56	STBY		NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP57	STBY	H-Z	IN VCORE_OV1	P/U 8.2K 3VDUAL	
GP58	STBY	H-Z	NATIVE F_USB_OC	P/U 8.2K 3VDUAL	
GP59	STBY		NATIVE USB_OC0#	N/A	
GP60	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	
GP61	STBY	L	NATIVE -SUSTAT	N/A	
GP62	STBY	L	NATIVE SUSCLK	N/A	
GP63	STBY	L	NATIVE GPIO63	N/A	
GP64	MAIN	L	NATIVE CLKOUTFLEX0	N/A	
GP65	MAIN	L	NATIVE CLKOUTFLEX1	N/A	
GP66	MAIN	L	NATIVE CLKOUTFLEX2	N/A	
GP67	MAIN	L	NATIVE CLKOUTFLEX3	N/A	
GP72	STBY	H-Z	NATIVE VCORE_OV4	P/U 8.2K 3VDUAL	
GP73	STBY		NATIVE 1_05V_OV1	P/U 8.2K 3VDUAL	
GP74	STBY	H-Z	NATIVE 1_05V_OV2	P/U 8.2K 3VDUAL	
GP75	STBY	H-Z	NATIVE N/A(Reverse)	P/U 8.2K 3VDUAL	

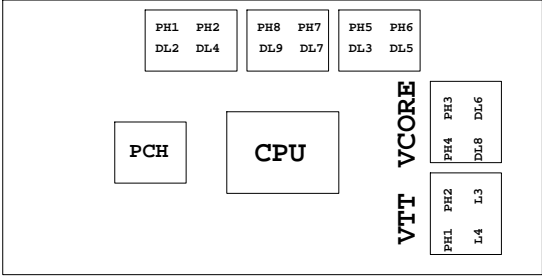
Super I/O ITE8720 GPIO Table

PIN NAME	USAGE	NOTE
SVC/PECI_RQT/GP14	-PECI_REQ	
PWROK1/GP13	PWROK1/ITE_PWROK	
KRST#/GP62	-KBRST	
SO/GP50	-ICH_SPI_CS	
IRTX/GP47/CE2_N/JP7	CEB_N	
GP46/IRRX	-LAN2_DSM	
PSION#/GP42	-PSON	
PWROK2#/GP41	PECI_CTL	
PCIRST3#/GP10/VDIMM_STR_EN	-PCIE_RST	
RSMRST#CIRRXL/GP55	-RSMRST	
PME#/GP54	-LPCPME	
PD5/GP75/BUSSO0	N/A	

PIN NAME	USAGE	NOTE
FAN_TAC2/GP52	FANIO2	
FAN_TAC3/GP37	FANIO3	
VIDO3/FAN_TAC4/GP25/DSR2#	FANIO4	
FAN_CTL2/GP51	FANPWM2	
FAN_CTL3/GP36	FANPWM3	
VID4/GP34	BEEP-	
VID3/GP33	TURBO1	
VID2/GP32	TURBO0	
VCORE_GOOD/VID6/GP63	CPUT_LED1_C	
VID5/GP35	CPUT_LED2_C	
VID1/GP31	CPUT_LED3_C	
VID0/GP30	-LAN1_DSM	NBT_LED1_C
SLCT/GP80	CPU_LED1_C	
PE/GP81	CPU_LED2_C	
BUSY/GP82	CPU_LED3_C	
PD3/GP73/BUSSI1	SB_LED1_C	
PD4/GP74/BUSSI2	SB_LED2_C	
VCORE_EN/VID7/GP64	IT_GP64	SB_LED3_C
PD0/GP70	NB_LED1_C	
PD1/GP71	NB_LED2_C	
PD2/GP72/BUSSIO	NB_LED3_C	
GP22/SCK	LOW_PWR_1	
VIDO5/GP27/SIN2	LOW_PWR_2	
PCIRST2#/GP11	-PFMRST1	
PCIRST1#/GP12	-PFMRST2	
3VSBSW#/GP40	CSI_F0	BSEL166_1
SUSC#/GP53	CSI_F1	BSEL166_2
GP23/SI	BSEL166_3/CSISBSL	
VIDO0/GP20/CTS2#	CPUT_LED1_C	BSEL166_4
GP65/VDDA_EN/GB_01	MB_ID2	
PD6/GP76/BUSSO1	MB_ID3	
PD7/GP77/BUSSO2	MB_ID4	
AFD#/GP86/SMBD_R	2X PIN	FST_2X8
INIT#/GP85/SMBD_M	SEC_2x8	GTLREF_AD2
ACK#/GP83	DDR_LED1_C	
VIDO1/GP21/DCD2#	DDR_LED2_C	
STB#/GP87/SMBC_M	DDR_LED3_C	
PWRON#GP44	VCORE_OV1	
PANSWH#/GP43	PWRBTSW	
KDAT/GP61	-PWRBTSW	
KCLK/GP60	KDAT	
MDAT/GP57	KCLK	
MACL/GP56	MDAT	
GP66/VLDT_EN/GB_02	NBT_LED1_C	MCLK
SVD/PCIRSTIN#/CIRTX/GP15	PWM2_CR	
KDAT/GP61	PWM2_CR	
GP67/CPU_PG/GB_03	EN_LOADLINE	IT_GP67/-EN_PWM2
SLIN#/GP84/SMBD_R	-EN_PWM2	
PSI_L/FAN_CLT5/CIRRXL2/GP16	-THERM	
VIDO4/GP26/SOUT2	DDR18V_PH2_EN	
VIDO2/FAN_TAC5/GP24/DSR2#	DDR18V_LED	
VIDO6/GP17/RI2#	1_1V_PH_EN	
VIDO7/JP6/DTR2#	JP6	
PD5/GP75/BUSSO0	SB_LED3_C	



PWM各相位的擺法如下：



BIOS超電壓對應表：

線路圖名稱	BIOS選項
Vcore	CPU Vcore
CPU_VTT	CPU Termination
CPU_VAXG	CPU Graphic Core
VCC1_8_PCH	CPU PLL
VCC1_05_PCH	PCH core
3VDUAL	3VDUAL
DDR15V	DRAM voltage
DDRVTT	DRAM Terminatio
VREF_CA_A/VREF_CA_B	DRAM Address Ref
VREF_DQ_A/VREF_DQ_B	DRAM Data Ref

散熱模組料號：

8IBP：
1.12SP2-01A001-Y1R/Y2R
2.12SP2-01A001-Z1R/Z2R
(HIBRID模組)包材階

	3 pin FAN control	4 pin FAN control	FAN speed	Controller
CPU FAN	FANPWM1	FANPWM3	FANIO1	IT8720
	ICH_FAN_PWM2	ICH_FAN_PWM0	ICH_FAN_TACH0	PCH
SYS FAN	FANPWM2	N/A	FANIO2	IT8720
	ICH_FAN_PWM1	N/A	ICH_FAN_TACH1	PCH
PWR FAN	N/A	N/A	FANIO3	IT8720
			ICH_FAN_TACH2	PCH

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